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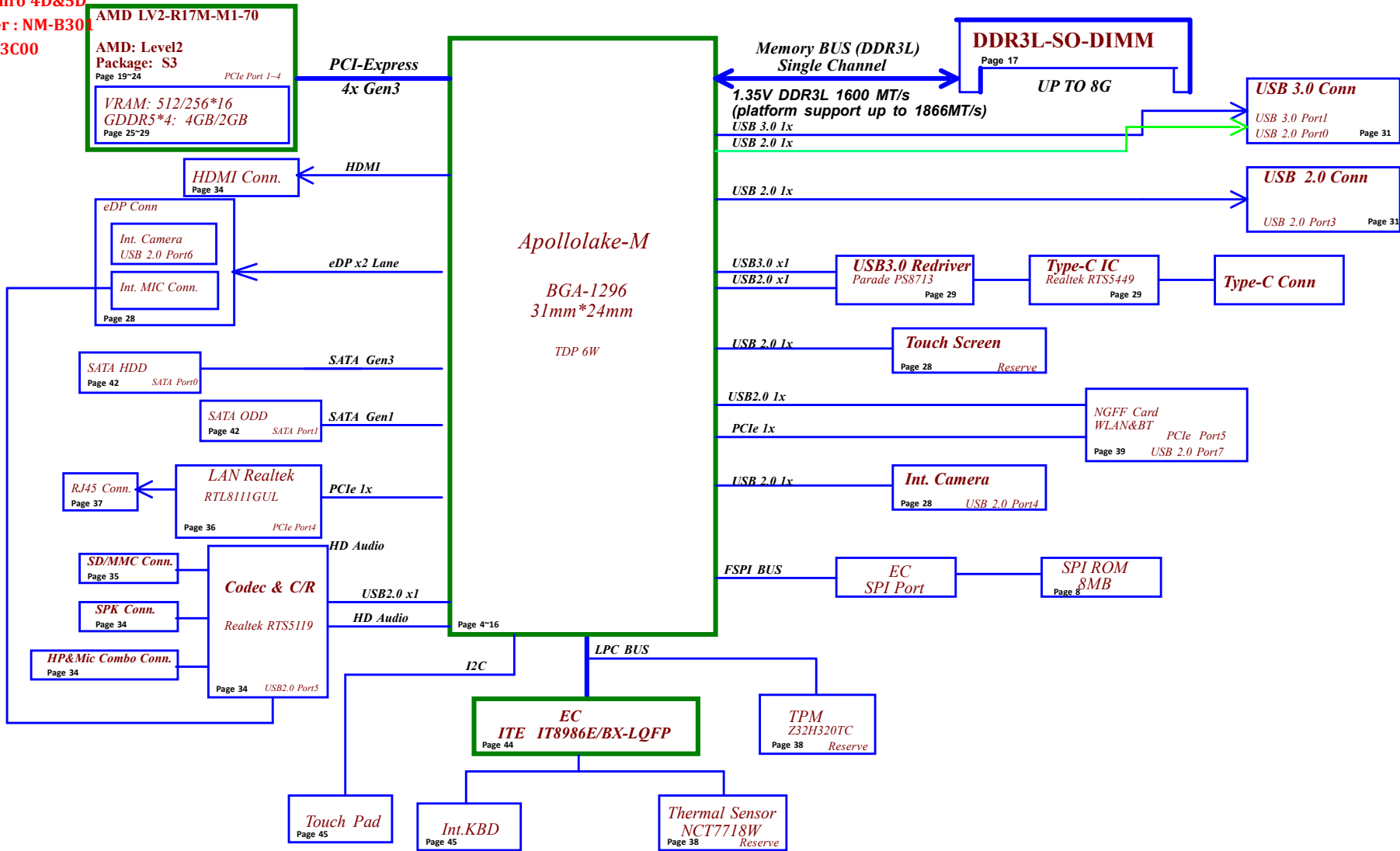
APL G 320 M/B DG424/DG524 Schematics Document Intel Apollolake M-Processor with DDRIII L + NV(AMD LV2-R17M-M1-70) GPU

2017-02-28

REV:1.0

Security Classification		LC Future Center Secret Data		Title	
Issued Date		2013/08/08		Deciphered Date	
				2014/01/21	
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				<small>Document Number</small> DG424/DG524	
				<small>Rev</small> 1.0	
<small>Date:</small> Thursday, March 09, 2017				<small>Sheet</small> 1 of 58	





Voltage Rails (0 --> Means ON , X --> Means OFF)

<div>Power Plane</div> <div>State</div>	V20B+ +3VL +5VL	+3VALW +5VALW	+3VALW_SOC +1.24VALW +1.8VALW	+1.35V	+5VS +3VS +1.8VS +1.05VS VTT +CPU_CORE +VNN
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

SMBUS Control Table

	SOURCE	VGA	BATT	IT8986HE	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	Charger	PMIC
EC_SMB_CK0 EC_SMB_DA0	EC +3VL	X	X	V	X	X	X	X	X	X	V
EC_SMB_CK1 EC_SMB_DA1	EC +3VL	X	V	V +3VL	X	X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	EC +3VS	V +3VGS	X	V +3VS	X	X	V	X	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_SOC	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X	X

EC SM Bus0 address		EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
PMIC	0x68	Smart Battery Charger	0x16 0x12	Thermal Sensor	0x98(reserve)	DDR SO-DIMM Wlan	0xA0 Rsvd

I2C4 Bus address (Touch Pad)

Device	Address
Slave	0x15
Descriptor	0x0001

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS/VTT	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
SOIX(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

XHCI	Port	Port device
USB 3.0	0	Type C
	1	USB3.0
USB 2.0	0	Type C(USB 2.0)
	1	USB3.0 (2.0)
	2	Touch Screen
	3	USB2.0
	4	Finger Print
	5	CARD READER
	6	CAMERA
	7	BT

DDI PORT LIST

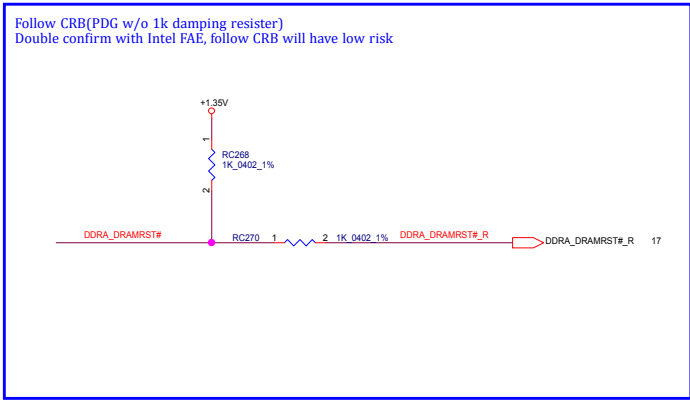
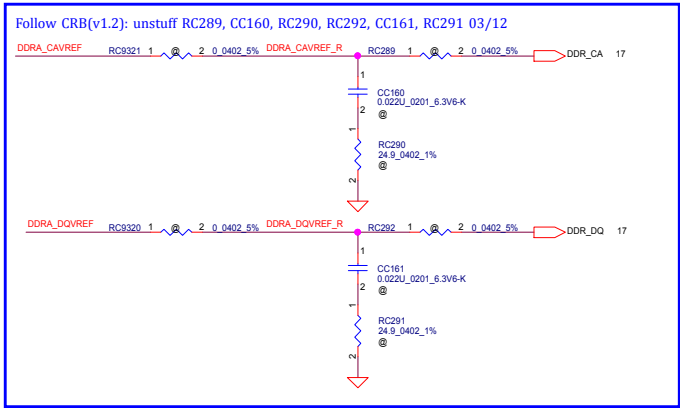
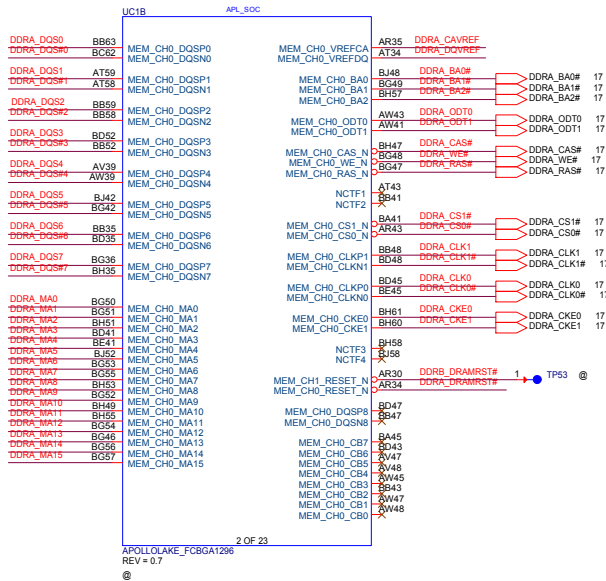
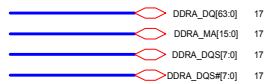
Port	Device
DDI0	NC
DDI1	HDMI
eDP	eDP

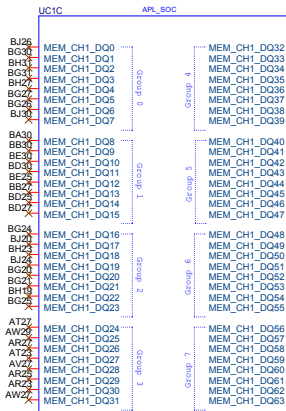
PCI PORT LIST

Port	Device	BIOS Device ID Map	CLK REQ
0	dGPU	PCIe1(Func0):Root Port#3	CLKREQ0
1			
2			
3	LAN	PCIe0(Func0):Root Port#1	CLKREQ1
4			
5	WLAN	PCIe0(Func1):Root Port#2	CLKREQ2

BOM Structure Table

BOM Structure	BTO Item
EMC@	For EMC part
EMC_NS@	For EMC un-stuff part
EMC_15@	EMC 15" part
EMC_14@	EMC 14" part
EMC_USB@	EMC USB TVS part
CD@	Cost Down part
RF@	For RF part
RF_NS@	For RF un-stuff part
RF_PXNS@	For RF GPU un-stuff part
14@	For 14" part
15@	For 15" part
8111GUL@	8111GUL LAN SKU part@
8111H@	8111H LAN SKU part@
PX@	Discrete GPU SKU part
TOPAZ@	TOPAZ dGPU SKU part
EXO@	R16M-M1-30 dGPU SKU part
UMA@	UMA SKU ID part
TMSEN@	Thermal Sensor part
TMSEN_PX@	dGPU Thermal Sensor part
TMSEN_UMA@	UMA Thermal Sensor part
TPM@	TPM part
NOVOTON@	NOVOTON TPM part
NATIONZ@	NATIONZ TPM part
TS@	Touch Screen part
FP@	Finger Print part
KBL@	KB Backlight part
UART@	UART debug part
RTCRST@	Clear RTCRST# function part
ME@	ME part
@	un-stuff part
HDMI@	HDMI Logo part
N3350_B0@	Apollolake N3350 B0 stepping QS CPU part
N3450_B0@	Apollolake N3450 B0 stepping QS CPU part
N4200_B0@	Apollolake N4200 B0 stepping QS CPU part
N3350_B1@	Apollolake N3350 B1 stepping MP CPU part
N3450_B1@	Apollolake N3450 B1 stepping MP CPU part
N4200_B1@	Apollolake N4200 B1 stepping MP CPU part
M2GX4@	Micron 2GB(256x16x4) VRAM X76 SKU
S2GX4@	Samsung 2GB(256x16x4) VRAM X76 SKU
H2GX4@	Hynix 2GB(256x16x4) VRAM X76 SKU
M2G@	Micron 2GB VRAM
S2G@	Samsung 2GB VRAM
H2G@	Hynix 2GB VRAM
PCB@	PCB part





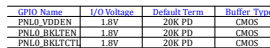
APOLLOLAKE_FCBGA1296
REV = 0.7
©



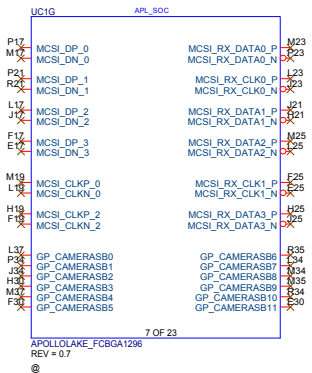
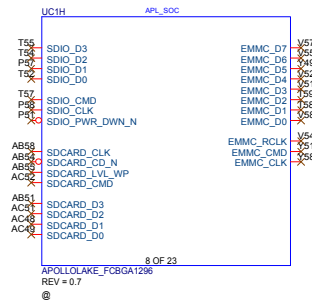
APOLLOLAKE_FCBGA1296
REV = 0.7
©



Port	Device	HPD Net	HPD Pin
DDI0	DP to VGA	VGA_HPD#	C50
DDI1	HDMI	HDMI_HPD#	A50
EDP	eDP	EDP_HPD#	P48



PCH_LCD_VDDEN_Q RC83 1 0 2 0 0402 5% **PCH_ENVDD** 28
PCH_LCD_VDDEN_Q VOH min is 1.35V
 SY6288C20 VIH min is 1.35V, do NOT use level shift
 (Follow BMWCI)
PCH_ENBKL 28
PCH_ENBKL can direct connect to EC for costdown



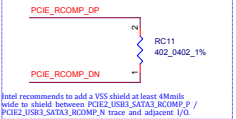
WLAN

LAN

dGPU

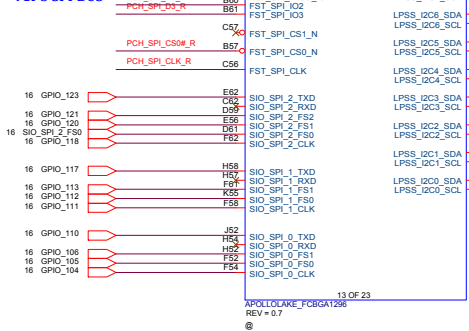
PCIE Configuration

Port	Config	Device	BIOS Device ID Map
P0			
P1			
P2	X4	dGPU	PCIe1(Func0):Root Port#3
P3			
P4	X1	LAN	PCIe0(Func0):Root Port#1
P5	X1	WLAN	PCIe0(Func1):Root Port#2

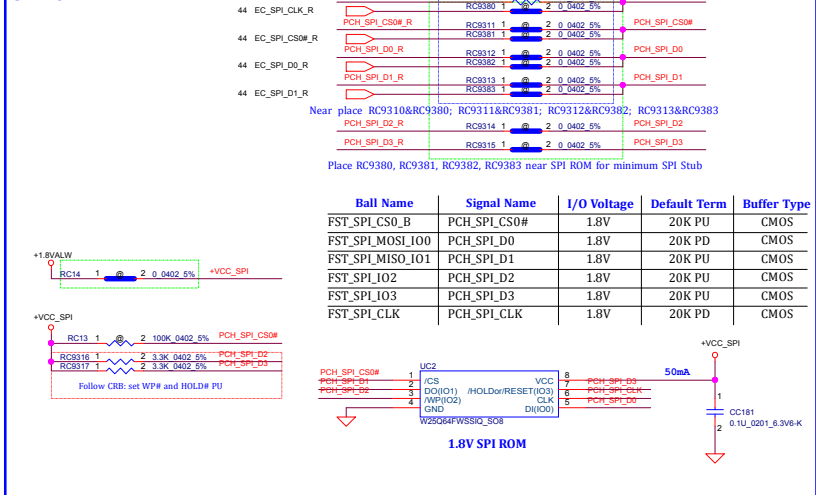


Intel recommends to add a VSS shield at least 4mm wide to shield between PCIE2_USB3_SATA3_ROMP_P / PCIE2_USB3_SATA3_ROMP_N trace and adjacent I/O

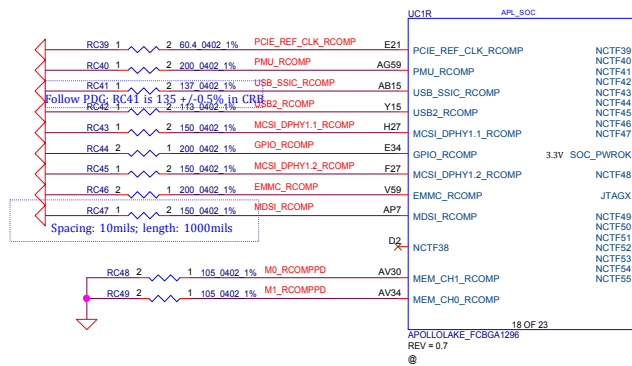
VIPB SPI BUS



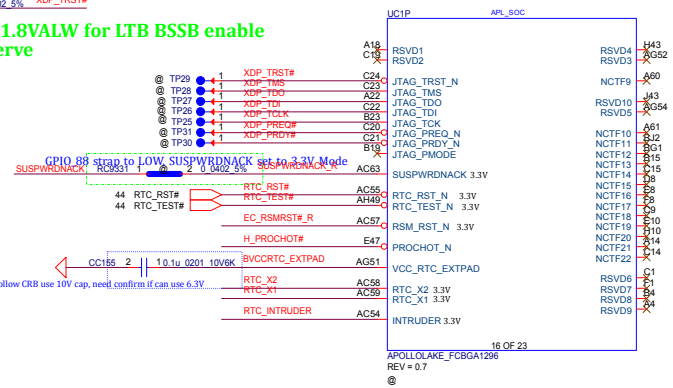
SPI ROM



The I2C signals are open drain, and it has internal pull-up.
A 1 kΩ ± 5% for external pull-up resistor is recommended.
Reserve Touch Pad I2C LS(MOS and IC) Lewis 2016/10/21

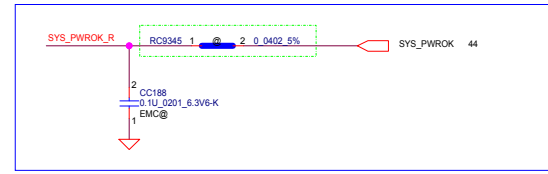
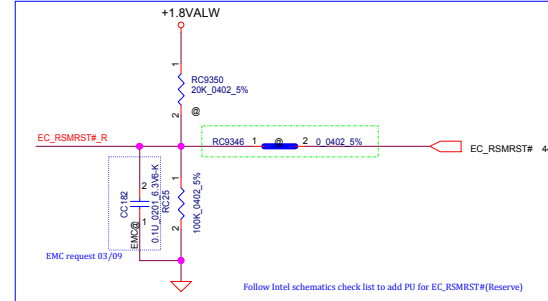
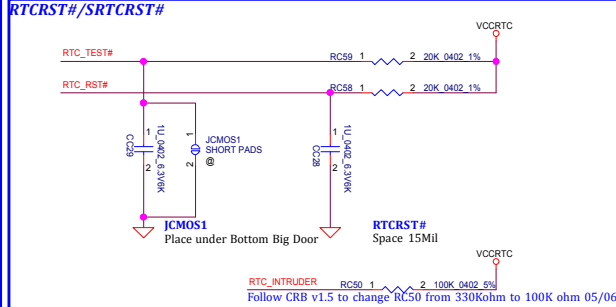
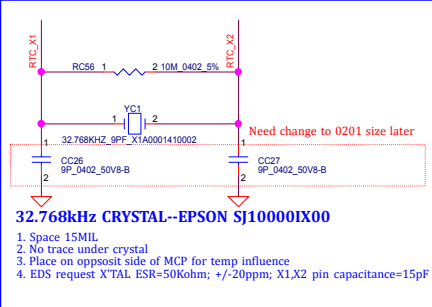


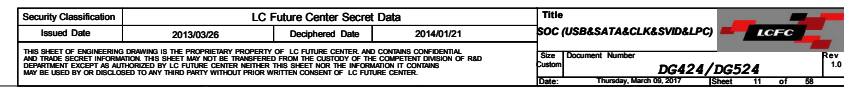
+1.8VALW
 use 10ohm pull up to +1.8VALW for LTB BSSB enable
 lewis 2016/10/21 reserve

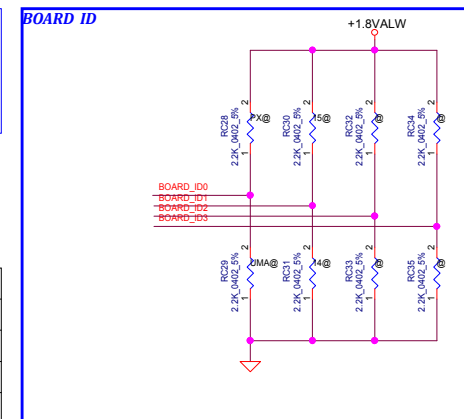
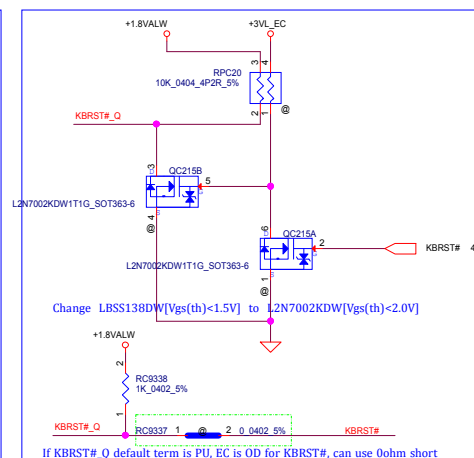
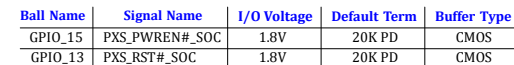



RCOMP RESISTOR REQUIREMENT

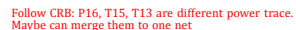
INTERFACE	PIN NAME	LOCATION	VALUE(ohm)
CSI1.1	MCSLDPHY1.1_RCOMP	RC43	150 +/-1%
CSI 1.2 (DPHY/CPHY)	MCSLDPHY1.2_RCOMP	RC45	150 +/-1%
USB2 and 3.3V mode GPIO	USB2_RCOMP	RC42	113 +/-1%
PCIe Refclk	PCIE_REF_CLK_RCOMP	RC39	60.4 +/-1%
modPHY (PCIe, USB3, SATA)	PCIE2_USB3_SATA3_RCOMP_P/N	RC11	402 +/-1%
MDSI	MDSI_RCOMP	RC47	150 +/-1%
SSIC	USB_SSIC_RCOMP	RC41	137 +/-1%
EMMC, Legacy and GPIO signals including 1.8V mode	EMMC_RCOMP	RC46	200 +/-1%
SD Card, PMU, LPC, SMBUS.	GPIO_RCOMP	RC44	
eDP	EDP_RCOMP_P/N	RC2	402 +/-1%
DDI	DDIO_RCOMP_P/N	RC1	402 +/-1%
Memory	MEM_CH0_RCOMP/MEM_CH1_RCOMP	RC49	105 +/-1%

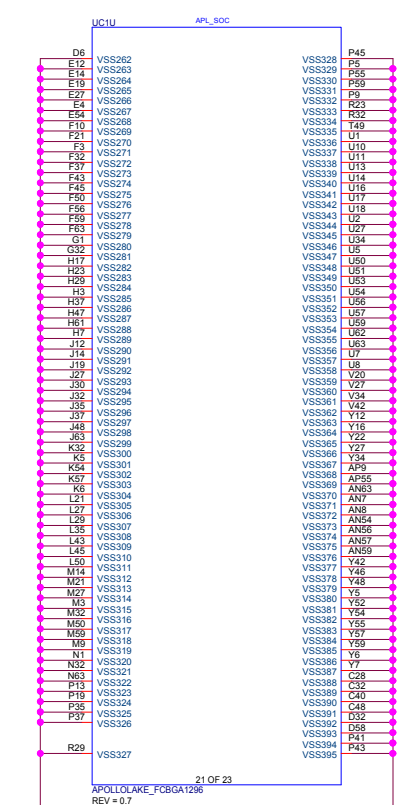
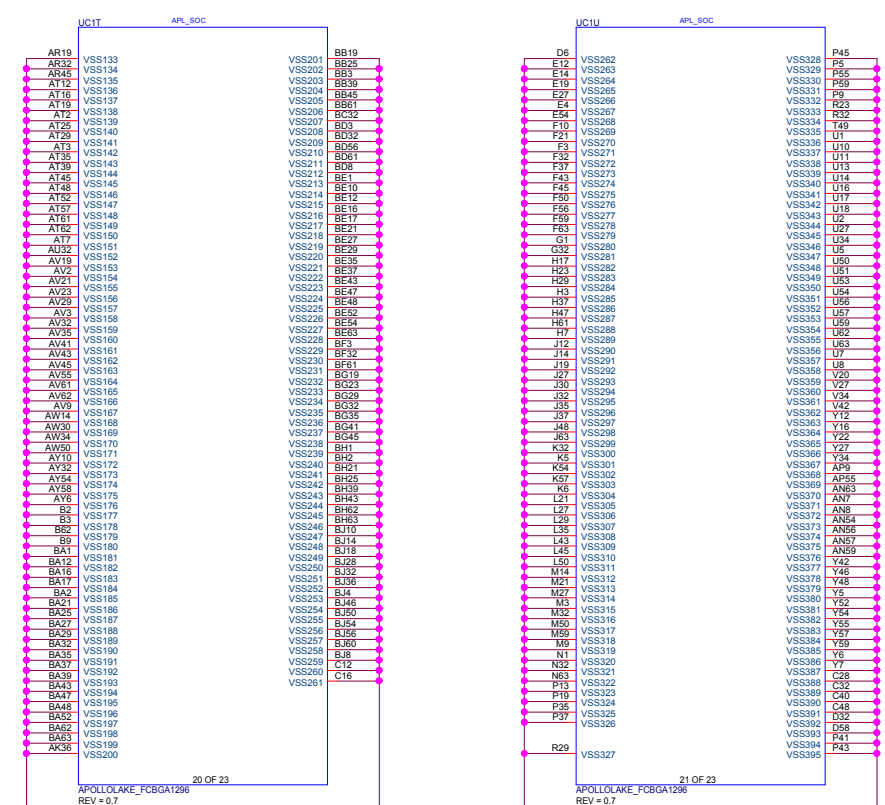
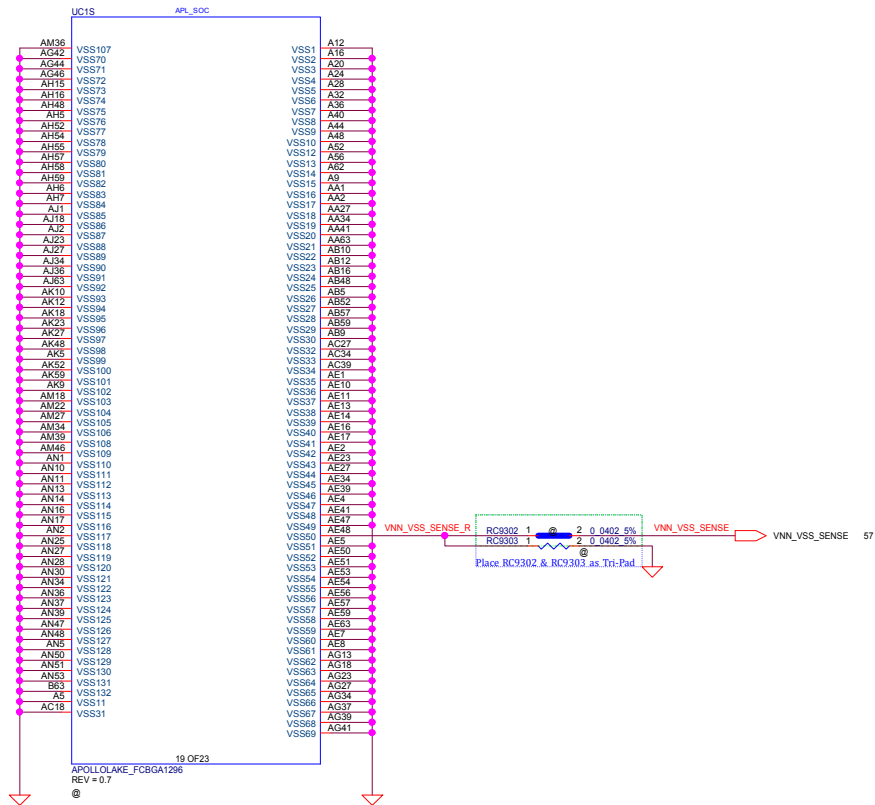




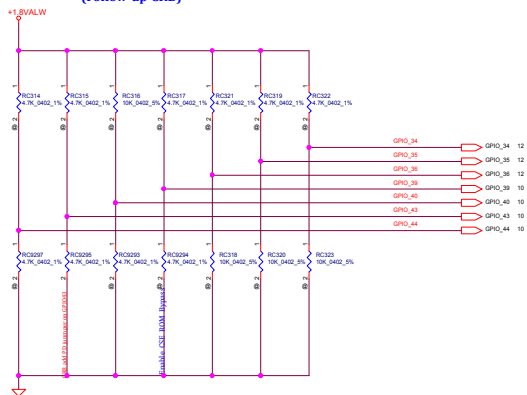


Security Classification		LC Future Center Secret Data		Title			
Issued Date		Deciphered Date		P12-SOC (GPIO&HDA)			
2013/08/08		2014/01/21					
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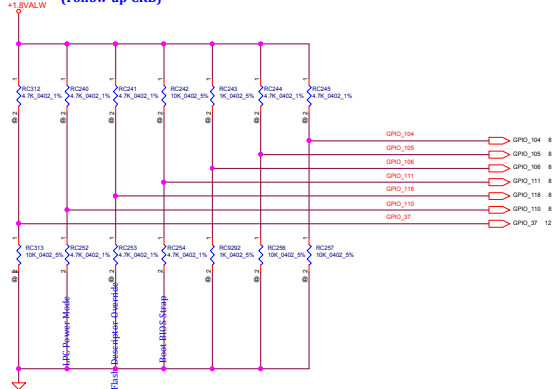




Hardware STRAPS (Follow up CRB)

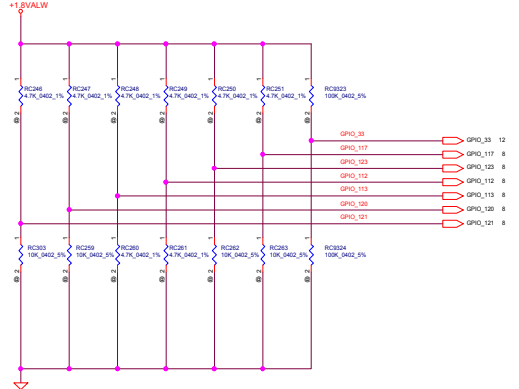
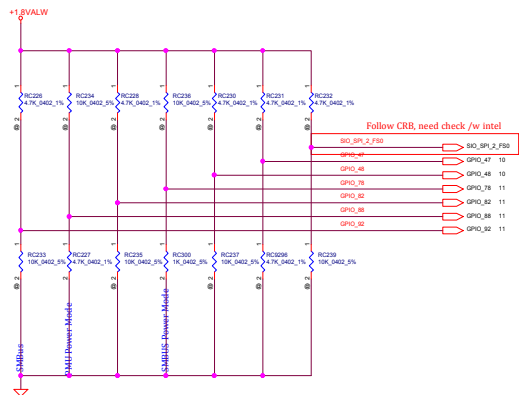
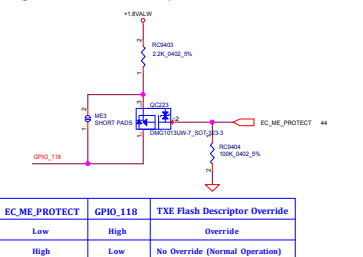


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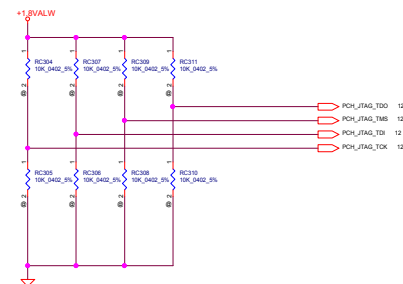


ME_PROTECT Circuit

Change to P-MOS Diodes DMC10131W7 09/02

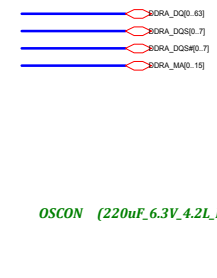


GPIO#	Purpose	Internal Termination	Schematics Setting	Pin usage	Remark
GPIO_33	RSVD	20K PD	Floating	N/A	Follow CRB(DOCh: 561386); EDS(v2.1) P54
GPIO_34	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v2.1) P47
GPIO_35	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v2.1) P47
GPIO_36	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v2.1) P47
GPIO_37	RSVD	20K PD	Floating	N/A	Follow CRB(DOCh: 561386); EDS(v1.5) P57
GPIO_39	Enable CSE ROM Bypass	20K PD	Floating	1 = Enable bypass 0 = Disable bypass (default)*	This strap tells CSE (TXE3.0) to bypass ROM EDS(v2.1) P47
GPIO_40	RTC Clock Timer Bypass	20K PD	Floating	1 = Enable bypass 0 = Disable bypass (default)*	Only be used when an external oscillator is used to supply a 32.768kHz clock to RTC_X1. EDS(v2.1) P47
GPIO_43	RSVD	20K PU	4.7K PD	Ensure this strap always PD for normal platform operation	EDS(v2.1) P47
GPIO_44	Allow SPI as a boot source	20K PU	Floating	1 = Enable(Default) 0 = Disable	EDS(v2.1) P47
GPIO_47	Force DNX FW Load	20K PD	Floating	1 = Force 0 = Do not force(Default)*	Recovery strap for corrupted FW image EDS(v2.1) P47
GPIO_48	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P47
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. SMBus signals are 3.3V mode. EDS(v2.1) P47
GPIO_82	RSVD	20K PD	Floating	Ensure this strap always PD for normal platform operation	EDS(v2.1) P47
GPIO_88	PMU 1.8V/3.3V mode select	20K PD	4.7K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. PMU signals are 3.3V mode. EDS(v2.1) P48
GPIO_92	SMBus No Re-Boot	20K PD	Floating	1 = Enable 0 = Disable(Default)*	Should strap this pin LOW. Functionality is handled by the PMC. EDS(v2.1) P48
GPIO_104	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_105	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_106	RSVD	20K PU	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	4.7K PD	1 = Buffers set to 1.8V mode(Default) 0 = Buffers set to 3.3V mode*	Follow CRB to strap this pin LOW. LPC signals are 3.3V mode. EDS(v3.1.1) P48
GPIO_111	RSVD	20K PU	4.7K PD	1 = Leave these regions unmapped by the System Agent 0 = Map these regions to the boot SPI	Pull LOW for designs that boot from SPI and HIGH otherwise. EDS(v2.1) P48
GPIO_112	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_113	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_117	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_118	Flash Descriptor Override	20K PD	4.7KPD	1 = Override 0 = No Override (Normal Operation)*	This strap enables the platform to override security features in the SPI. EDS(v2.1) P48
GPIO_120	Top swap override	20K PD	Floating	1 = Enable 0 = Disable (default)*	This strap enables platform to change different SPI ROM location. ESD(v2.1) P48
GPIO_121	RSVD	20K PD	Floating	Ensure this strap is PD when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48
GPIO_123	RSVD	20K PU	Floating	Ensure this strap is PU when RSM_RST_N de-asserts for normal platform operation	EDS(v2.1) P48

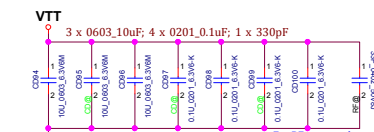
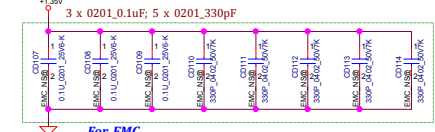
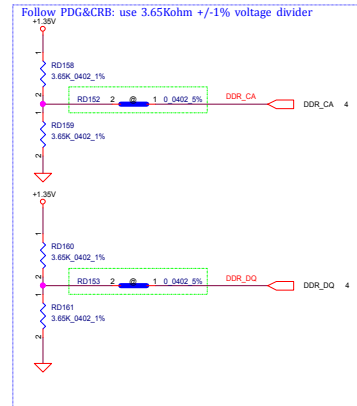



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DRAA DQ00---DQ01
DRAA DQ01---DQ02
DRAA DQ02---DQ03
DRAA DQ03---DQ04
DRAA DQ04---DQ05
DRAA DQ05---DQ06
DRAA DQ06---DQ07
DRAA DQ07---DQ08
DRAA DQ08---DQ09
DRAA DQ09---DQ10
DRAA DQ10---DQ11
DRAA DQ11---DQ12
DRAA DQ12---DQ13
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DRAA DQ284---DQ285
DRAA DQ285---DQ286
DRA
```



Layout Note:
Place near DIMM



For RF request: keep 0402 and set to mount



0.65000.727

Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		Blank	
2013/08/08		2013/08/05			
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LCFC

1.0

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μ s.

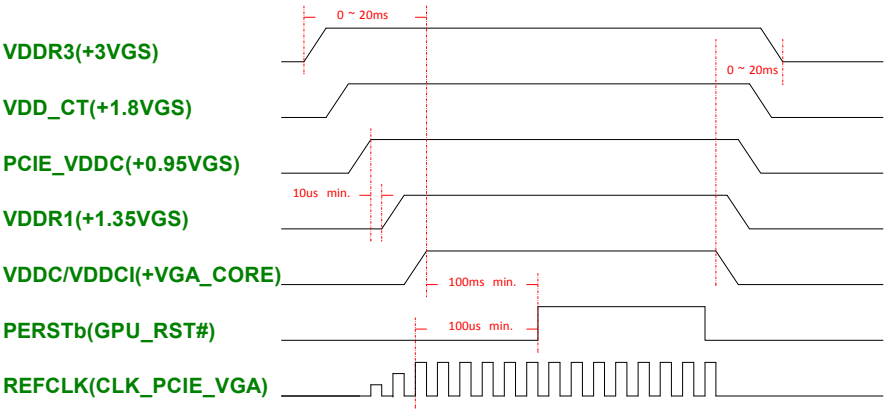
It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU.

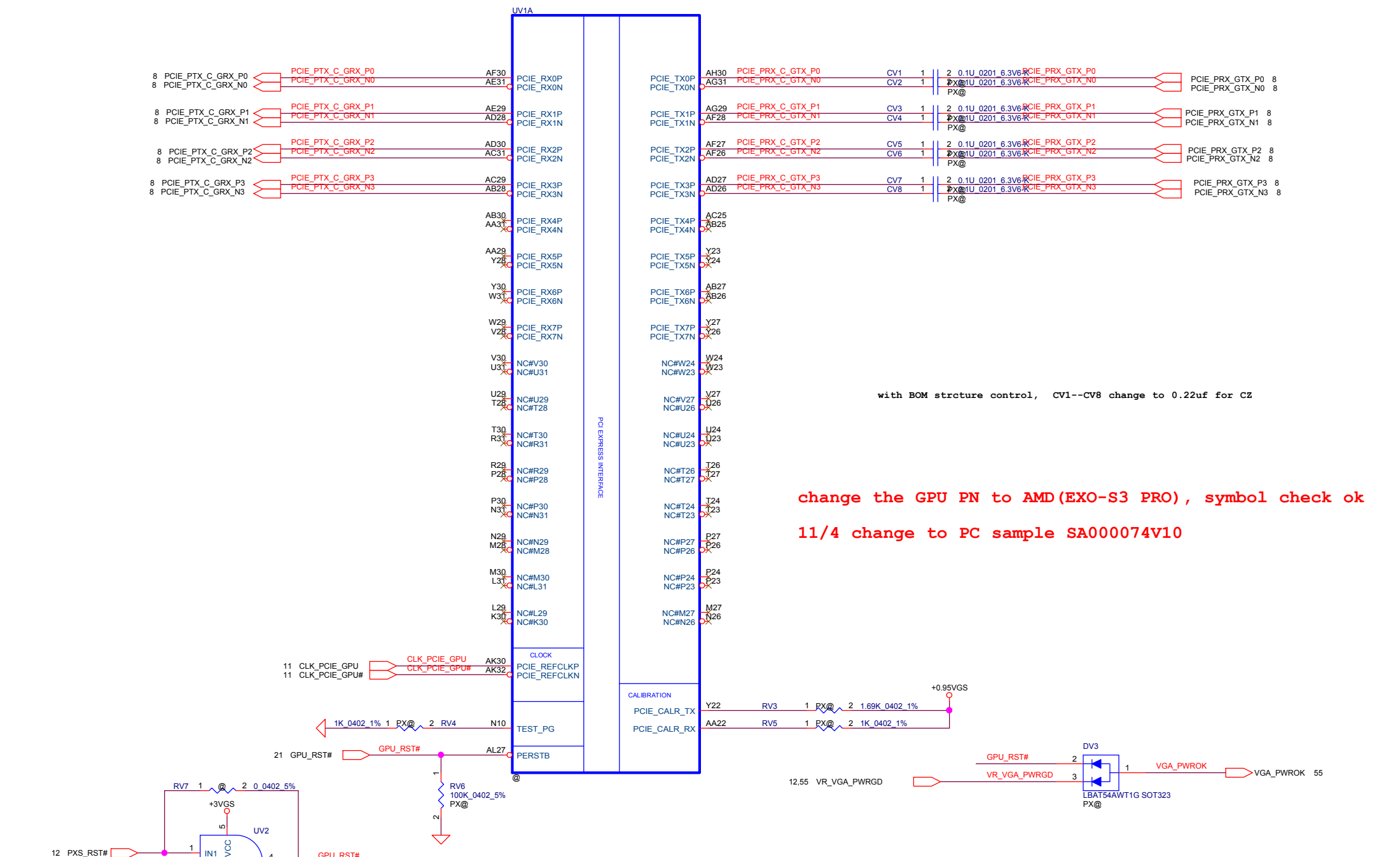
The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μ s)

For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx16	Hynix H5GC4H24AJR-R0C	100	4.53K	4.99K
	Micron EDW4032BABG-70-F	111	4.75K	NC
	Samsung K4G41325FE-HC28	110	3.4K	10K
		000	NC	4.75K
		010	4.53K	2K
		001	8.45K	2K

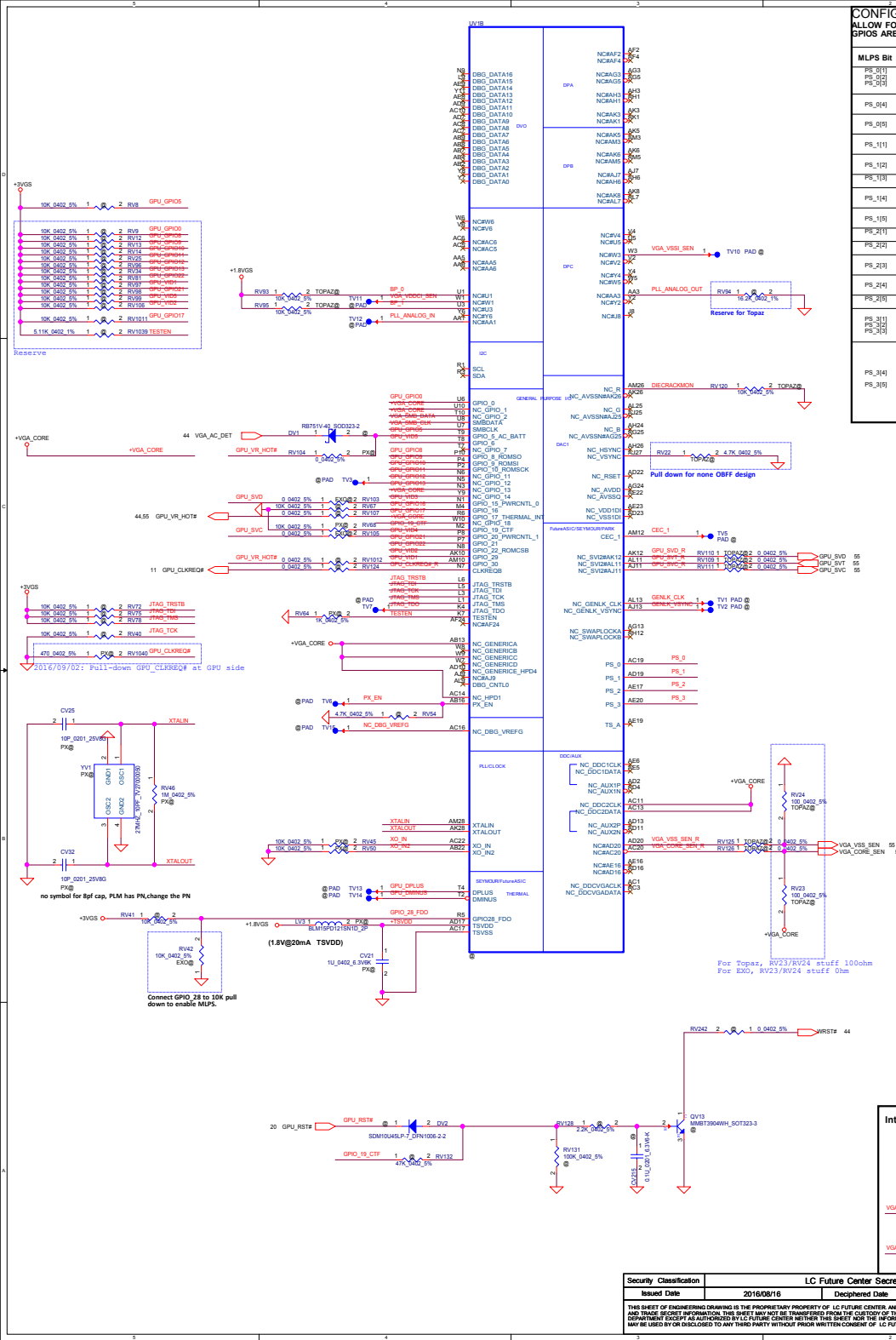


with BOM strcture control, CV1--CV8 change to 0.22uf for CZ

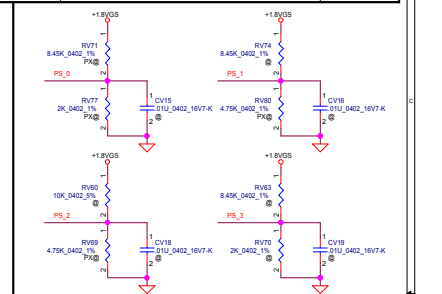
change the GPU PN to AMD(EXO-S3 PRO) , symbol check ok

11/4 change to PC sample SA000074V10

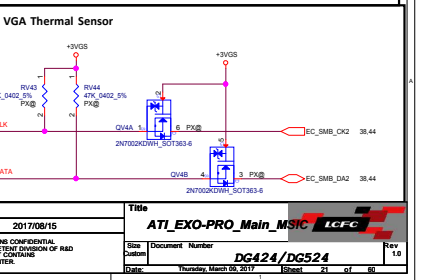
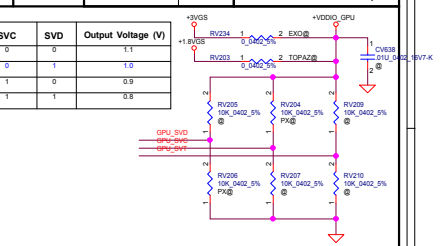
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	ATI_EXO-PRO_PCIE	
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				DG424/DG524	
				Date:	Thursday, March 09, 2017
				Sheet	20 of 58
				Rev	1.0



CONFIGURATION STRAPS				
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE STRAPS ARE USED, THEY MUST NOT CONFLICT DURING RESET				
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS	
PS_0[1]	ROM_CONFIG[1]	Define the ROM type when STRAP_BIOS_ROM_EN = 1		x
PS_0[2]	ROM_CONFIG[2]	Define the primary memory output size when STRAP_BIOS_ROM_EN = 0	001 = 256MB	
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.		1
PS_0[5]	AUD_PORT_CONFN_PFNSTRAP[5]	The USB (least significant bit) of the strap option that indicates the number of auto-capable display outputs.		1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported 0 = PCIe GEN3 is not supported.	1= GEN3 is supported	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQ power management capability is disabled 1 = The CLKREQ power management capability is enabled		0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter full-swing is enabled 1 = The transmitter full-swing is disabled		1
PS_1[5]	STRAP_TX_CFG_DEMPEH_EN	0 = Tx deemphasis disabled 1 = Tx deemphasis enabled	1= Enable	x
PS_2[1]	N/A	Reserved.		0
PS_2[2]	N/A	Reserved.		0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0= Disable	x
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capability disabled 1 = The device will not be recognized as the system's VGA controller		1
PS_2[5]	N/A	Reserved.		0
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strap, such as for memory ID	100 = Hynix 1G 111 = Micron 1G 101 = Samsung 1G	x
PS_3[2]	BOARD_CONFIG[1]	Board configuration related strap, such as for memory ID	000 = All endpoints are usable.	
PS_3[3]	BOARD_CONFIG[2]	Board configuration related strap, such as for memory ID	111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	11



MLPS	Bit			BOM		
	5	4	3	2	1	0
PS_0 [5:1]	1	1	0	0	1	RV71=8.45K
PS_1 [5:1]	1	1	0	0	1	RV74=8.45K
PS_2 [5:1]	1	1	0	0	1	RV60=NC
PS_3 [5:1]	1	1	1	1	1	RV63=NC
PS_4 [5:1]	1	1	1	1	1	RV63=NC
PS_5 [5:1]	1	1	1	1	1	RV63=NC
PS_6 [5:1]	1	1	1	1	1	RV63=NC
PS_7 [5:1]	1	1	1	1	1	RV63=NC
PS_8 [5:1]	1	1	1	1	1	RV63=NC
PS_9 [5:1]	1	1	1	1	1	RV63=NC
PS_10 [5:1]	1	1	1	1	1	RV63=NC
PS_11 [5:1]	1	1	1	1	1	RV63=NC
PS_12 [5:1]	1	1	1	1	1	RV63=NC
PS_13 [5:1]	1	1	1	1	1	RV63=NC
PS_14 [5:1]	1	1	1	1	1	RV63=NC
PS_15 [5:1]	1	1	1	1	1	RV63=NC
PS_16 [5:1]	1	1	1	1	1	RV63=NC
PS_17 [5:1]	1	1	1	1	1	RV63=NC
PS_18 [5:1]	1	1	1	1	1	RV63=NC
PS_19 [5:1]	1	1	1	1	1	RV63=NC
PS_20 [5:1]	1	1	1	1	1	RV63=NC
PS_21 [5:1]	1	1	1	1	1	RV63=NC
PS_22 [5:1]	1	1	1	1	1	RV63=NC
PS_23 [5:1]	1	1	1	1	1	RV63=NC
PS_24 [5:1]	1	1	1	1	1	RV63=NC
PS_25 [5:1]	1	1	1	1	1	RV63=NC
PS_26 [5:1]	1	1	1	1	1	RV63=NC
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PS_84 [5:1]	1	1	1	1	1	RV63=NC
PS_85 [5:1]	1	1	1	1	1	RV63=NC
PS_86 [5:1]	1	1	1	1	1	RV63=NC
PS_87 [5:1]	1	1	1	1	1	RV63=NC
PS_88 [5:1]	1	1	1	1	1	RV63=NC
PS_89 [5:1]	1	1	1	1	1	RV63=NC
PS_90 [5:1]	1	1	1	1	1	RV63=NC
PS_91 [5:1]	1	1	1	1	1	RV63=NC
PS_92 [5:1]	1	1	1	1	1	RV63=NC
PS_93 [5:1]	1	1	1	1	1	RV63=NC
PS_94 [5:1]	1	1	1	1	1	RV63=NC
PS_95 [5:1]	1	1	1	1	1	RV63=NC
PS_96 [5:1]	1	1	1	1	1	RV63=NC
PS_97 [5:1]	1	1	1	1	1	RV63=NC
PS_98 [5:1]	1	1	1	1	1	RV63=NC
PS_99 [5:1]	1	1	1	1	1	RV63=NC
PS_100 [5:1]	1	1	1	1	1	RV63=NC



UV1F

NC_VARY_BL
NC_DIGON

AB11
AB12

+VGA_CORE

NC_UPHYAB_TMDPA_TX0N
NC_UPHYAB_TMDPA_TX0P

ΔL15
ΔK14

NC_UPHYAB_TMDPA_TX1N
NC_UPHYAB_TMDPA_TX1P

ΔH16
ΔJ15

NC_UPHYAB_TMDPA_TX2N
NC_UPHYAB_TMDPA_TX2P

ΔL17
ΔK16

NC_UPHYAB_TMDPA_TX3N
NC_UPHYAB_TMDPA_TX3P

ΔH18
ΔJ17

NC_TXOUT_L3P
NC_TXOUT_L3N

ΔL19
ΔK18

TMDP

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NC_UPHYAB_TMDPB_TX0P

ΔH20
ΔJ19

NC_UPHYAB_TMDPB_TX1N
NC_UPHYAB_TMDPB_TX1P

ΔL21
ΔK20

NC_UPHYAB_TMDPB_TX2N
NC_UPHYAB_TMDPB_TX2P

ΔH22
ΔJ21

NC_UPHYAB_TMDPB_TX3N
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ΔL23
ΔK22

NC_TXOUT_U3P
NC_TXOUT_U3N

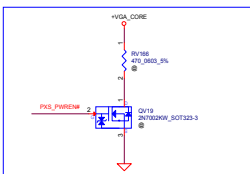
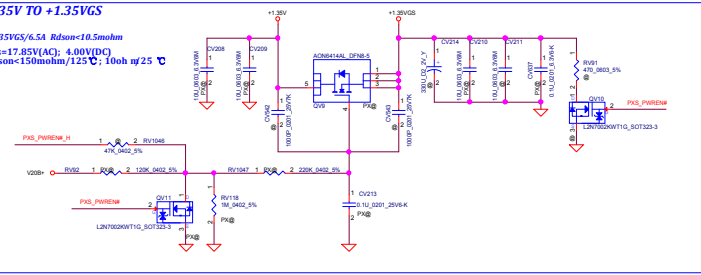
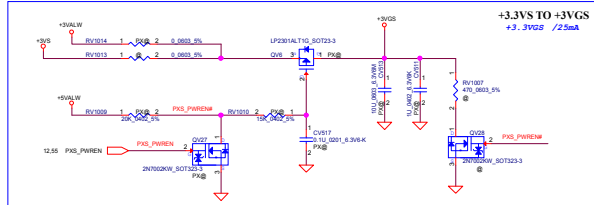
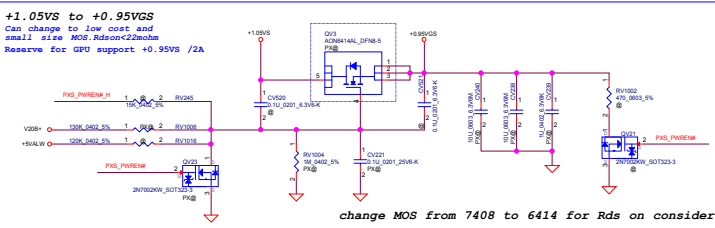
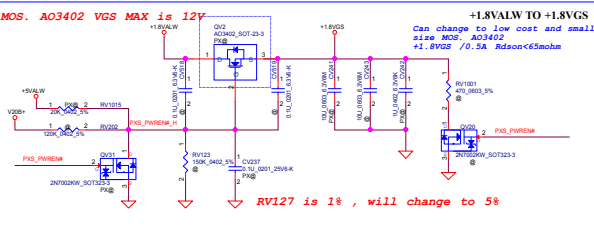
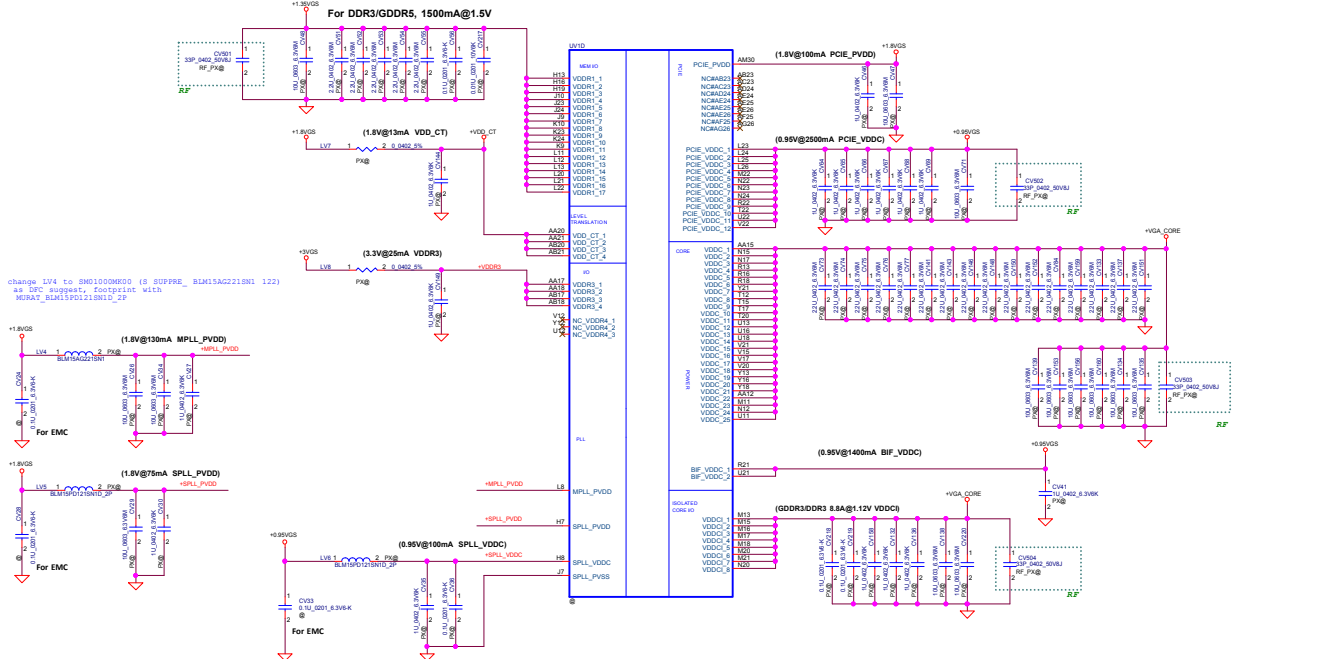
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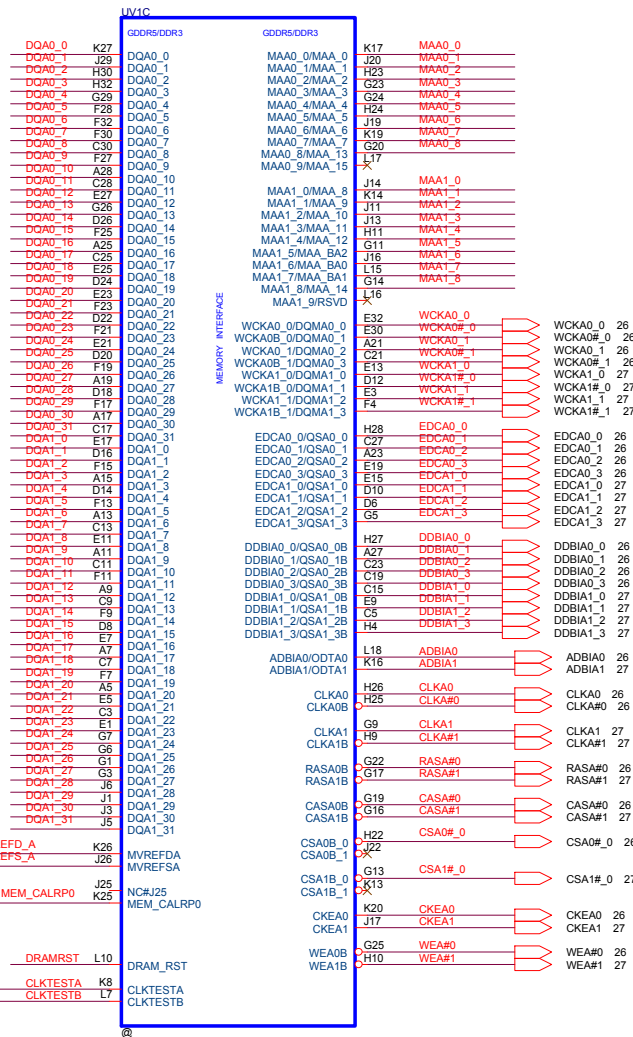
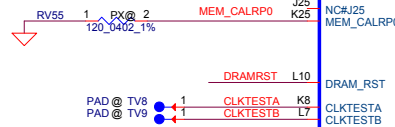
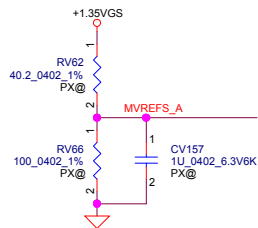
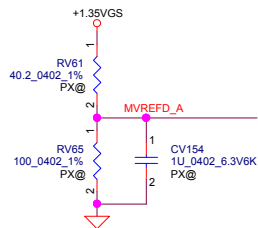
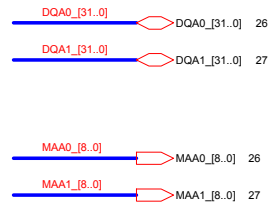
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Issued Date	2016/08/16	Deciphered Date	2017/08/15	ATI_EXO-PRO_TMDP	
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				Date:	Thursday, March 09, 2017
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				Rev	1.0



change LV4 to 8M1000K000 (S SUPPRE, BLK15AG221SN1 122)
as 32C suggest, output with
MERAT, BLK15PD121SN10_21






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								DG424/DG524	
Date:				Thursday, March 09, 2017				Sheet 25 of 60	

 DQA0_[31..0] 25
 MAA0_[8..0] 25

MF=1 Mirror

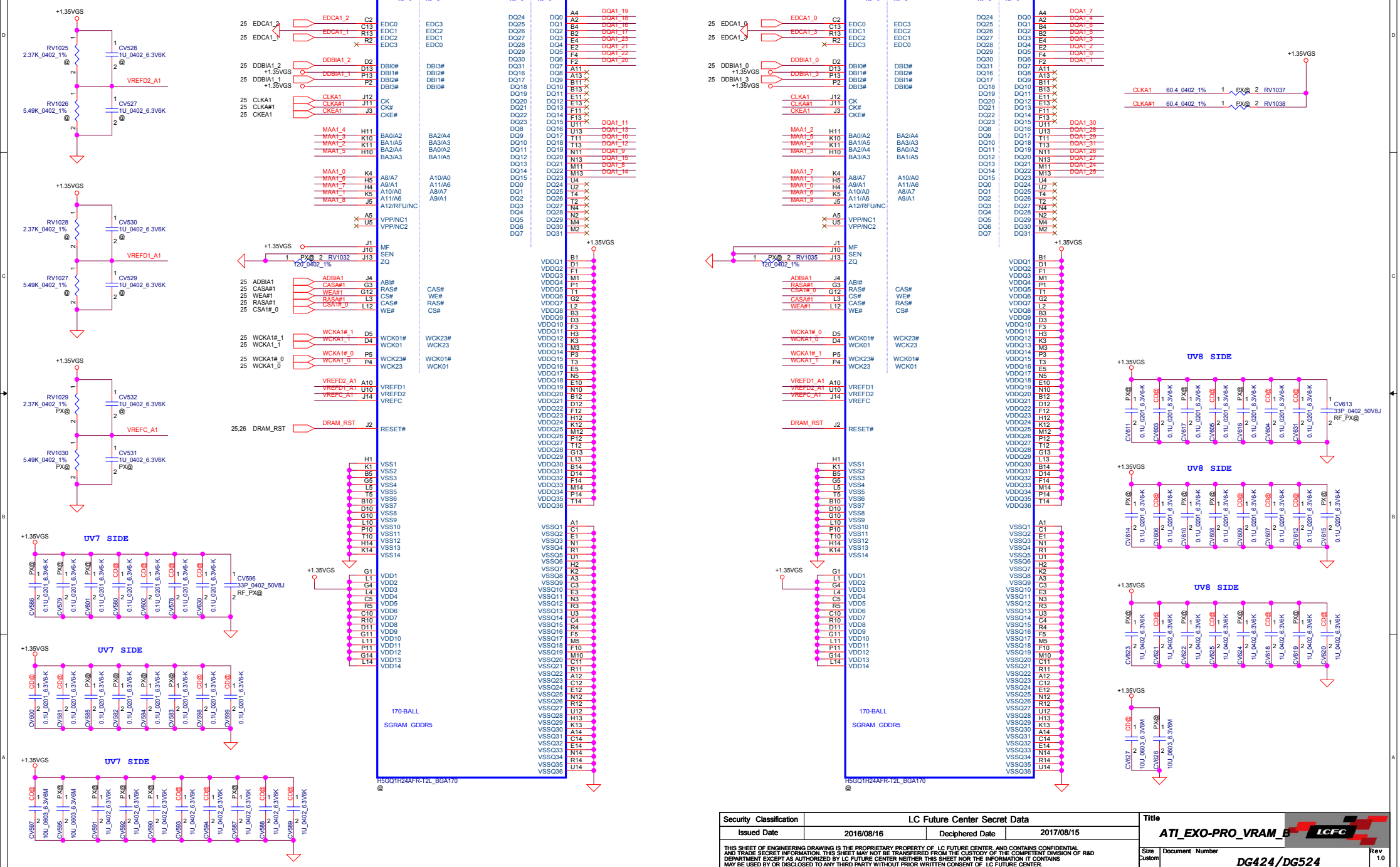



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	ATI_EXO-PRO_VRAM_A 	
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				Date:	Thursday, March 09, 2017, 13:26 26 of 60

 DQA1_[31..0] 25
 MAA1_[8..0] 25

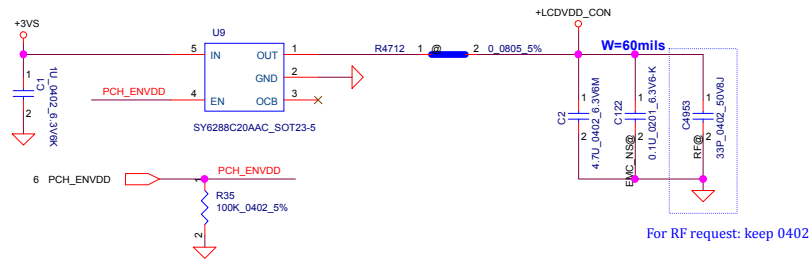
UV7			
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UV8			
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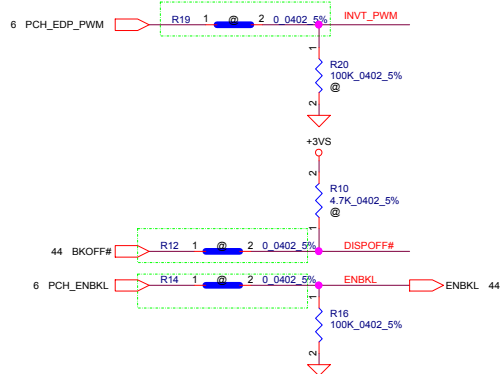


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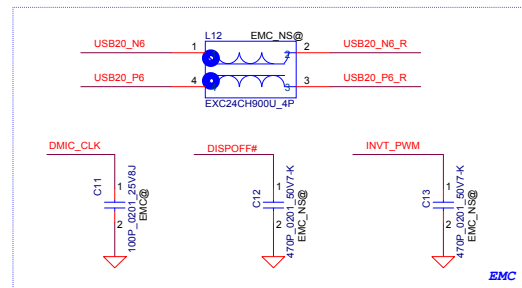
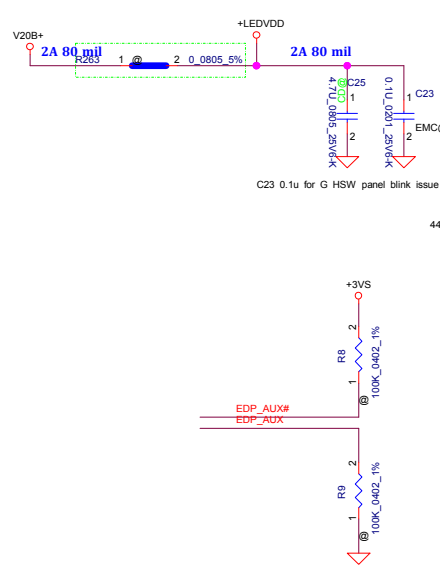
LCD POWER CIRCUIT



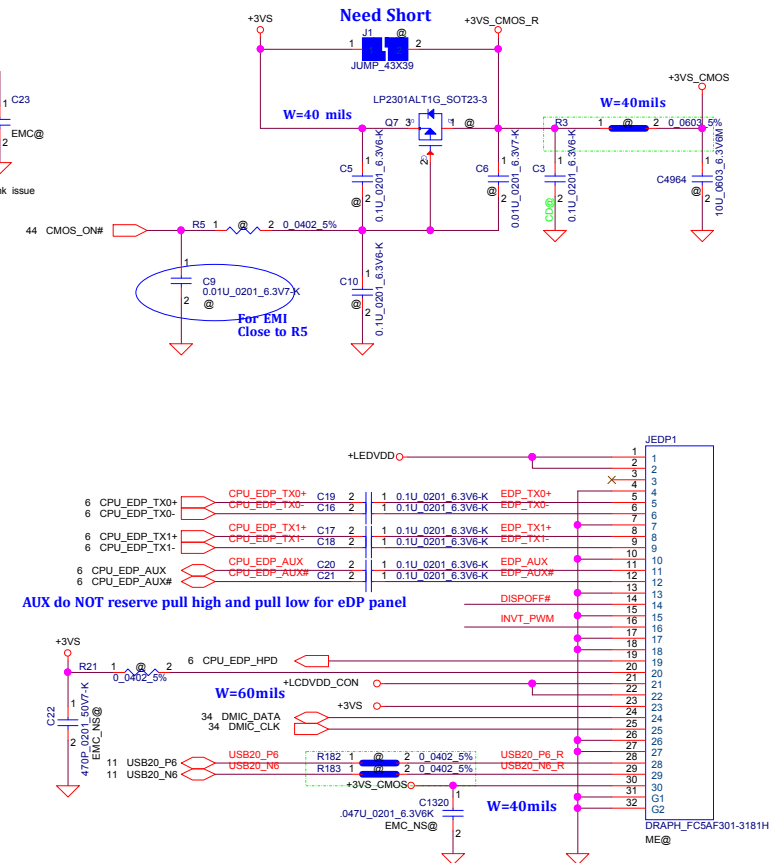
APL SoC output enable Voh min is 1.8V-0.45V=1.35V



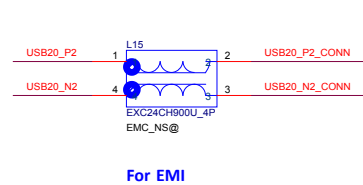
B+ to +LEDVDD POWER



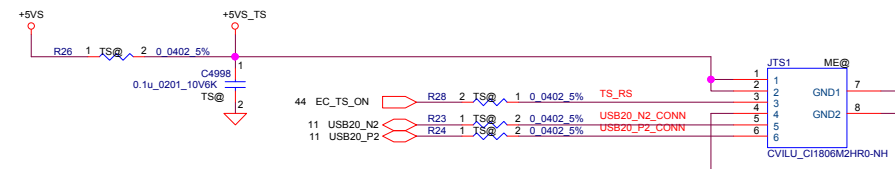
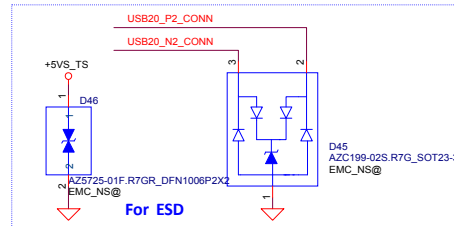
CMOS CAMERA




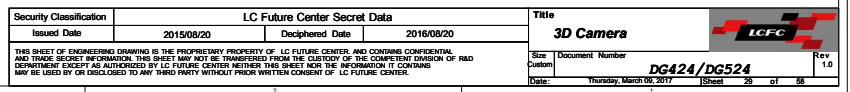
Touch Screen



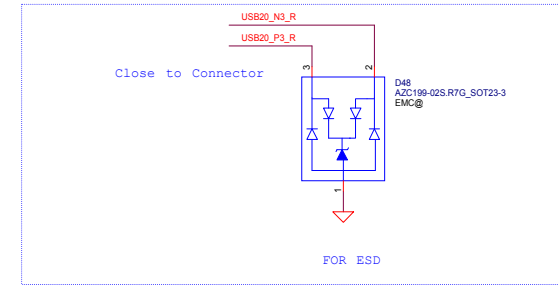
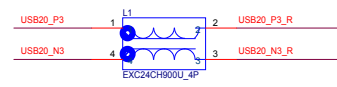
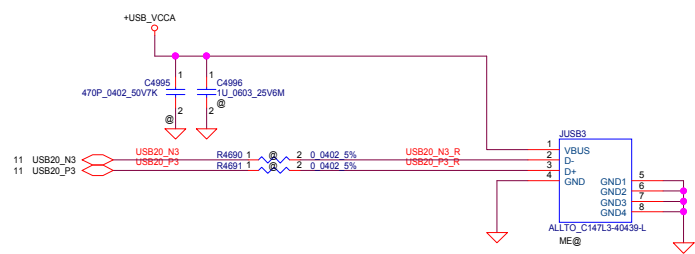
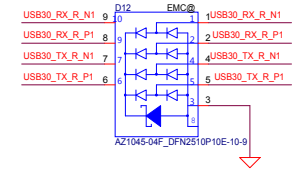
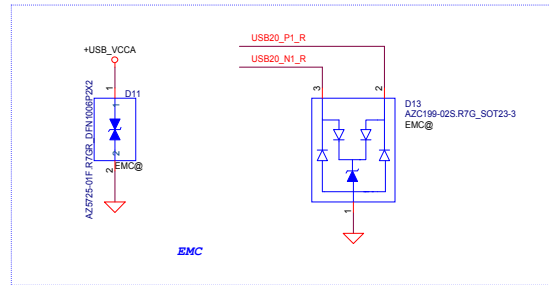
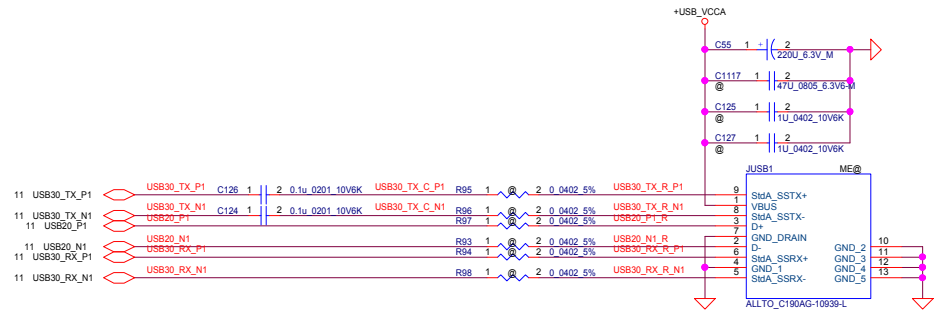
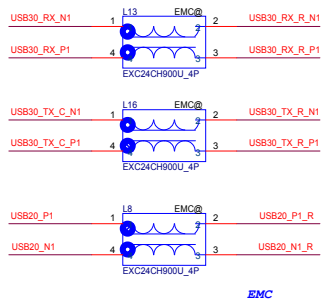
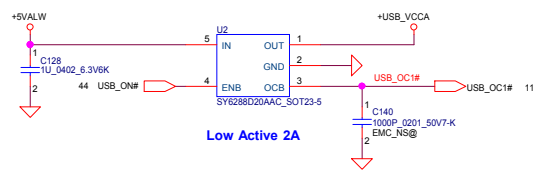
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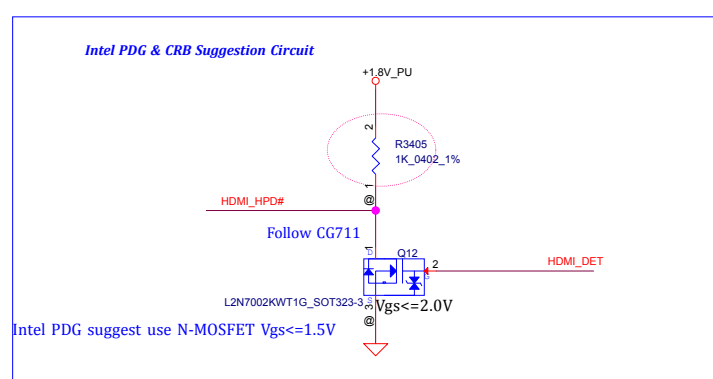
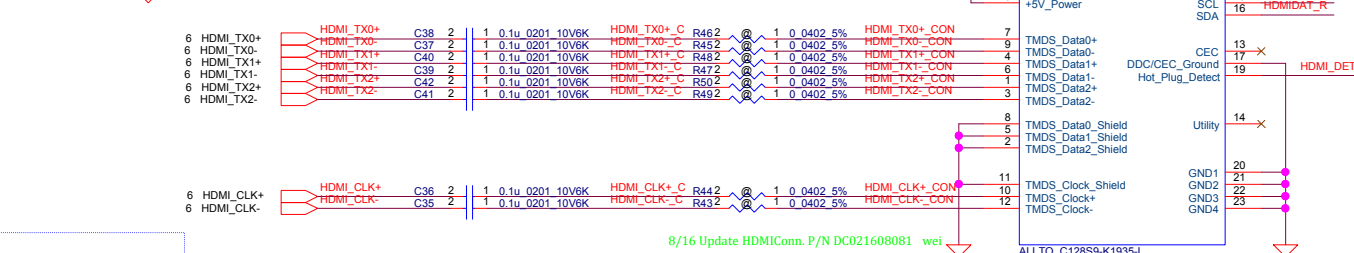
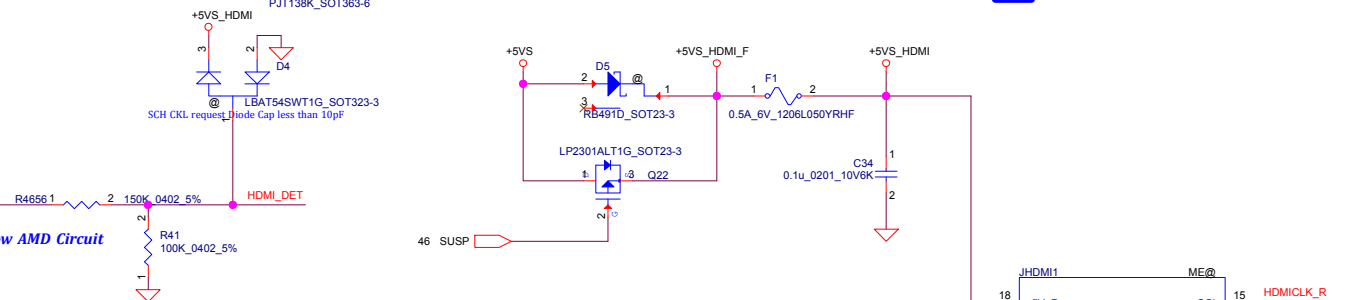
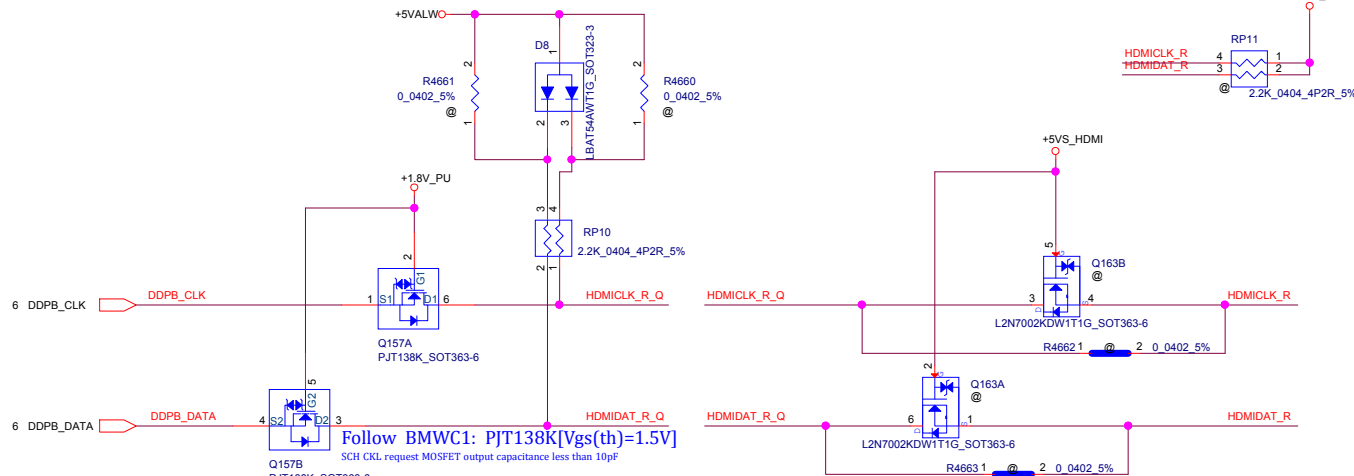
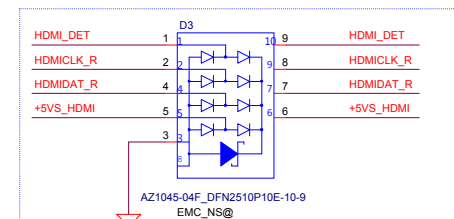
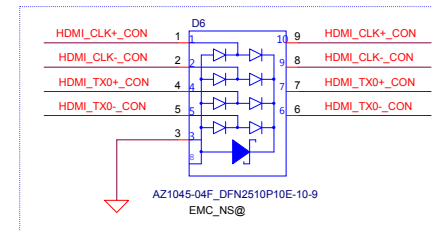
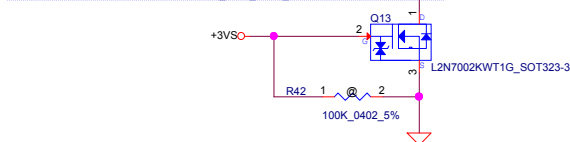
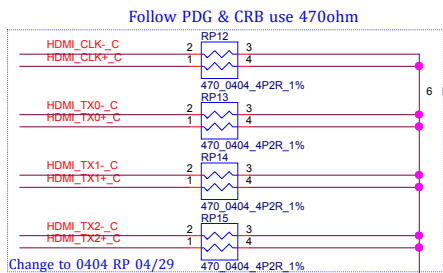
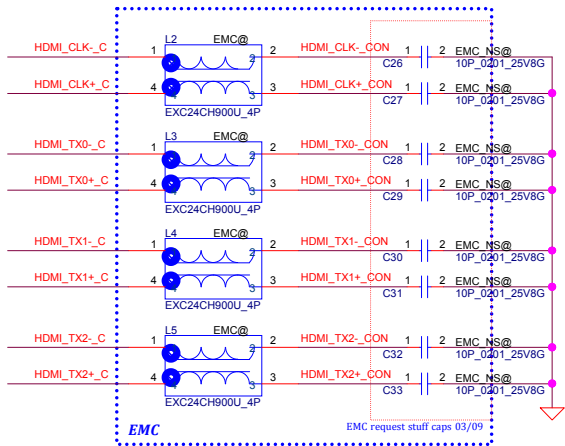


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				Date:	Thursday, March 09, 2017	Sheet 28 of 58 Rev 1.0

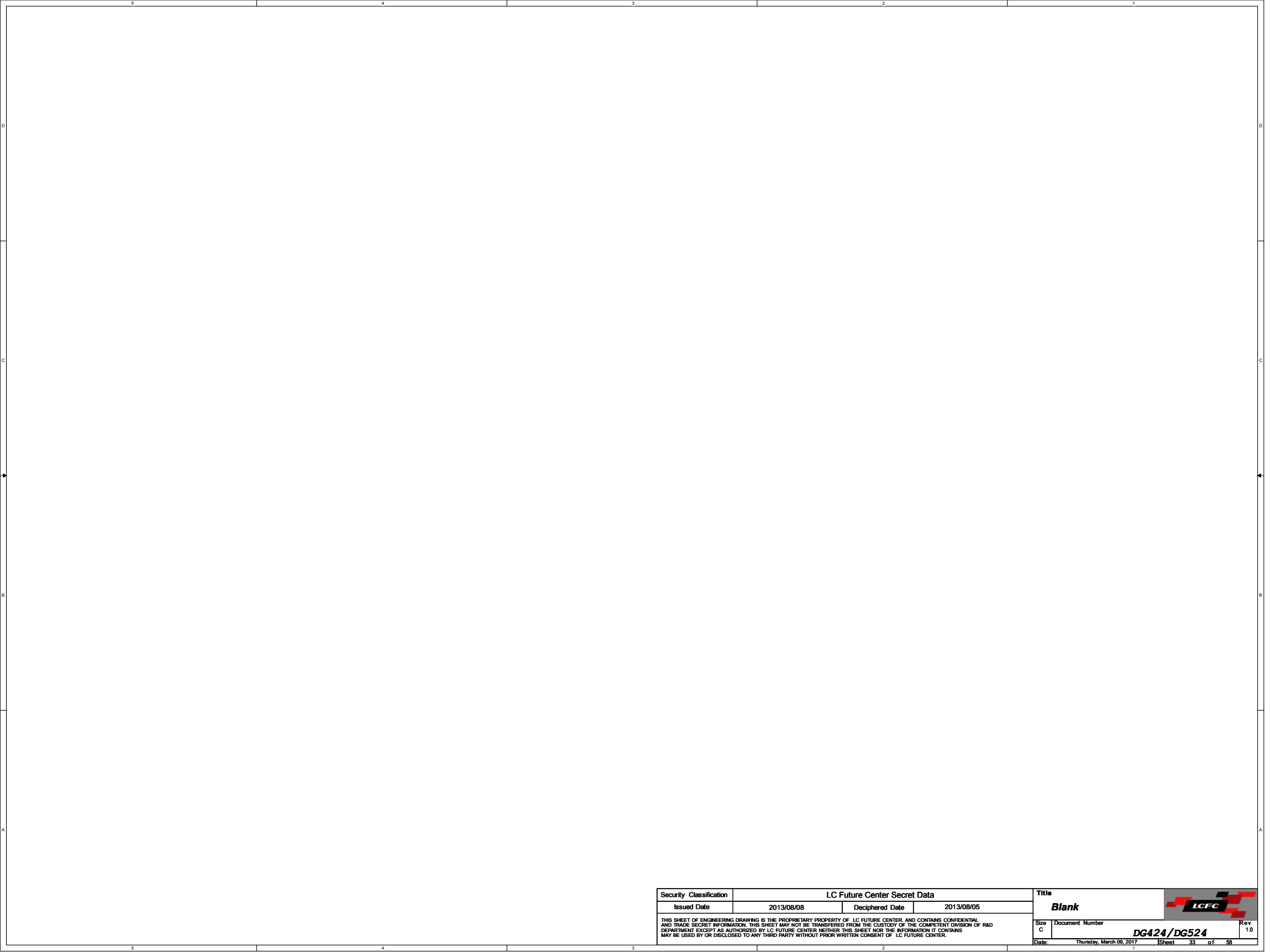


USB3.0 Port X 1




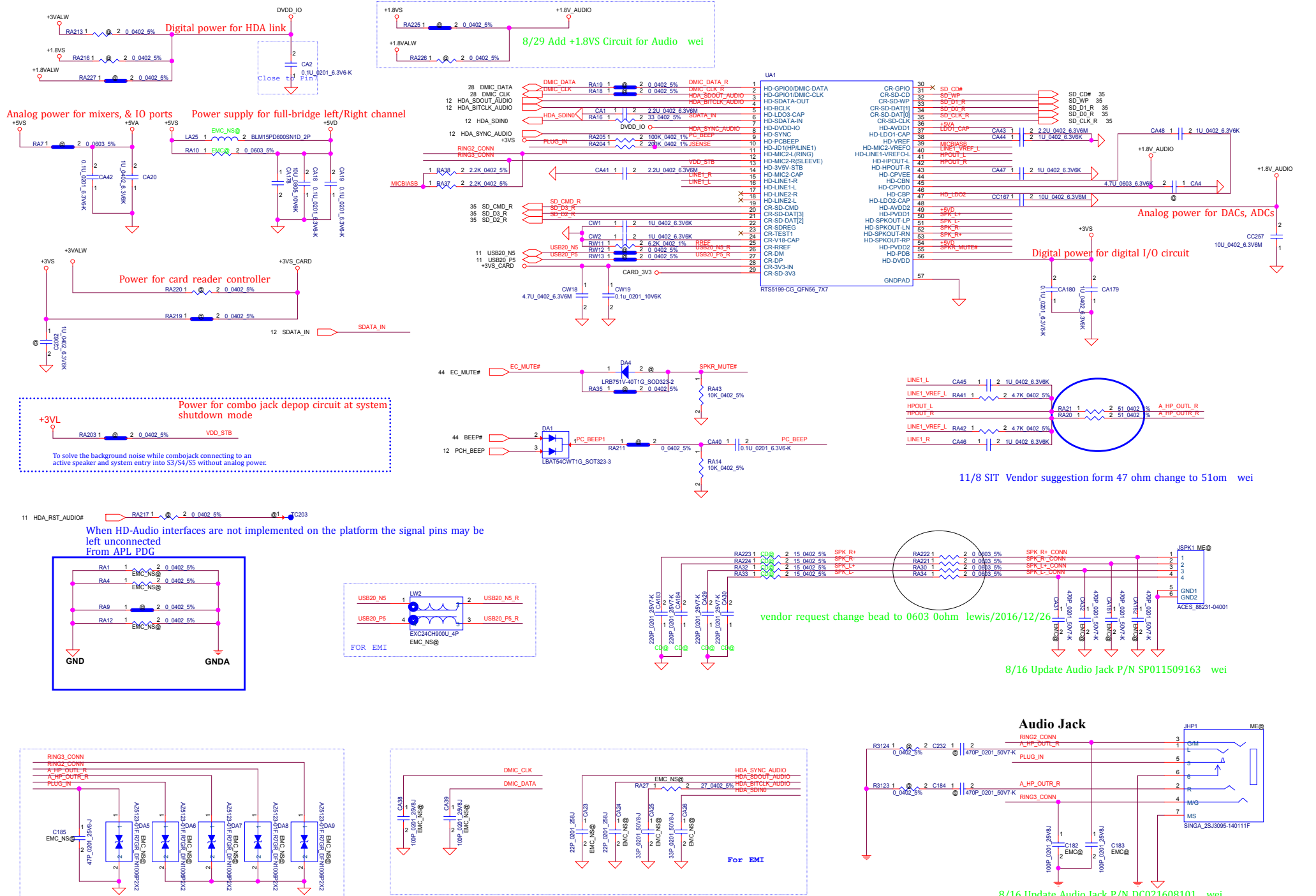


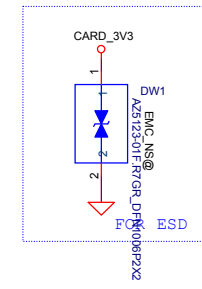
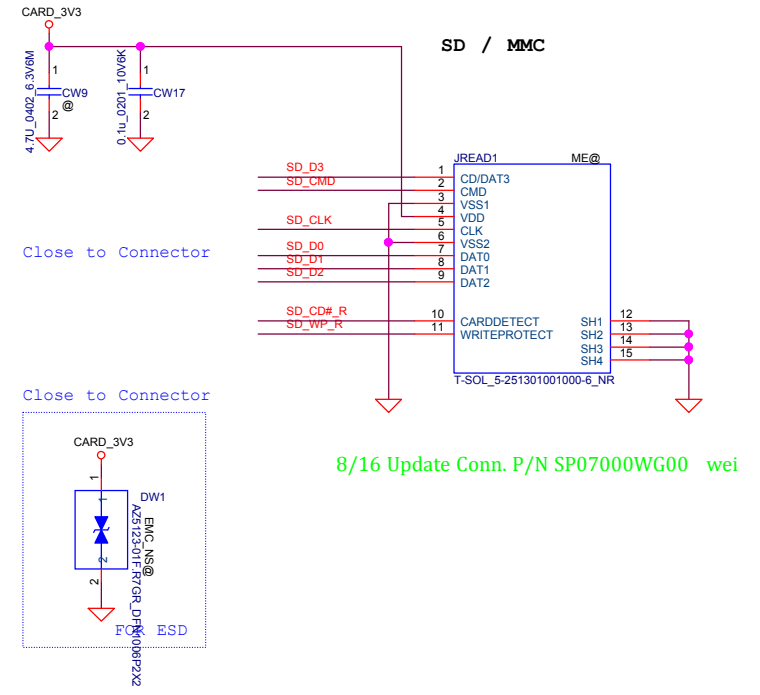
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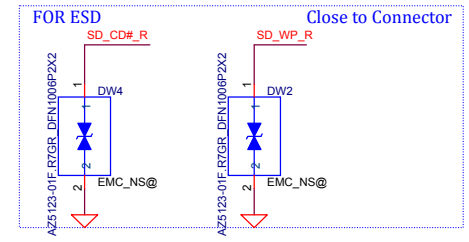
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Issued Date		2013/08/08		Deciphered Date	
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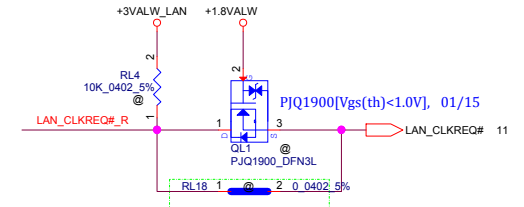
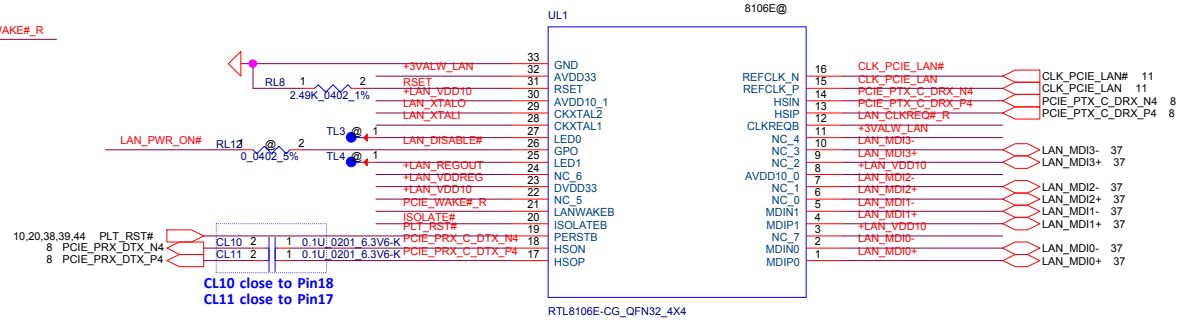
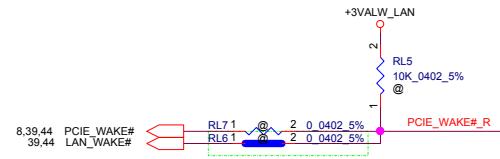
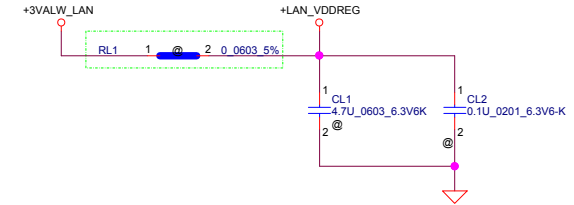
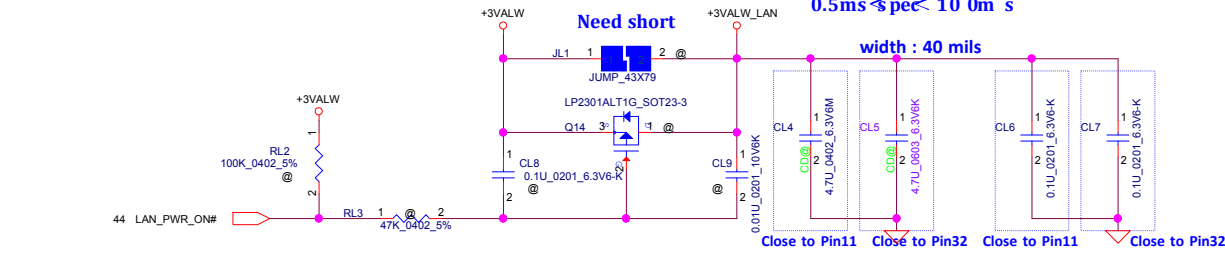


8/16 Update Conn. P/N SP07000WG00 wei

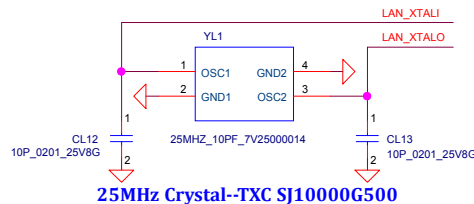
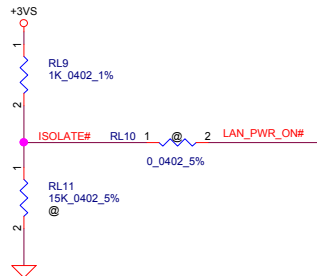


+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
 $0.5\text{ms} \leq t_{\text{pec}} \leq 100\text{ms}$

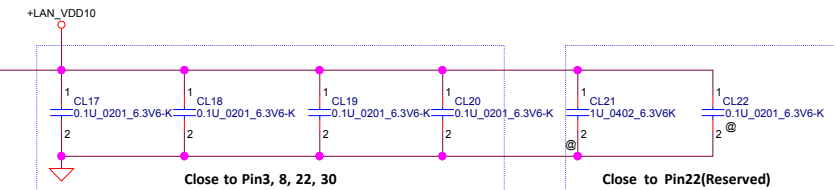
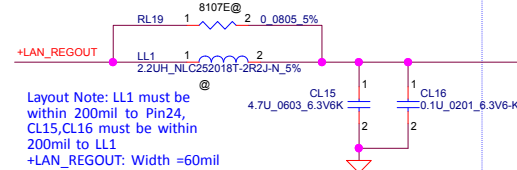


APL SOC CLKREQ are 1.8VALW power plane



Follow common pool change 25MHz X'tal from EPSON to TXC. 03/01

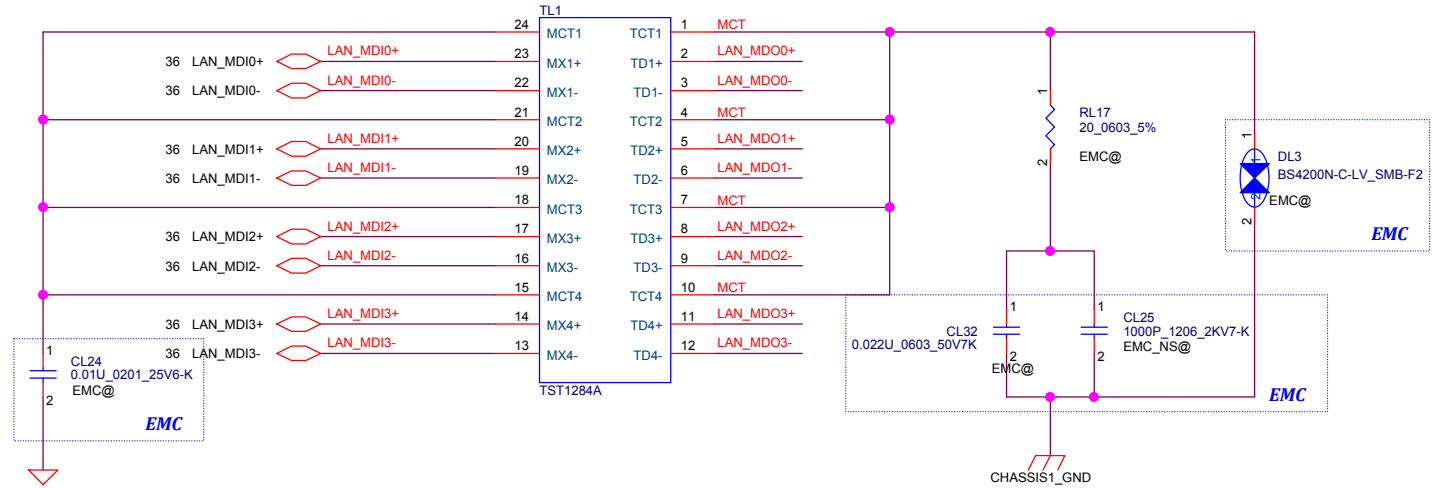
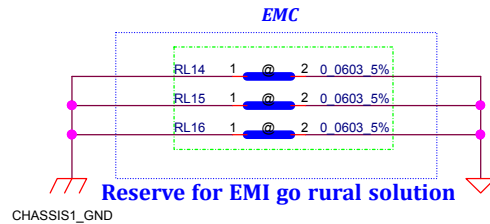
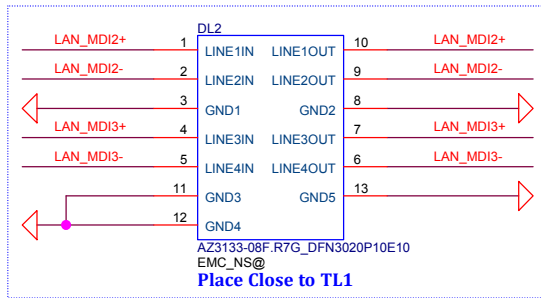
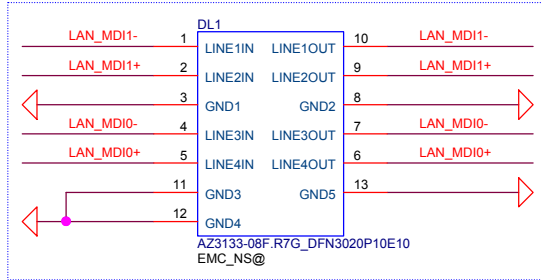
For RTL8111GUL SWR mode)
For RTL8111H /RTL 8107E (LDO mode) RL19 stuf f



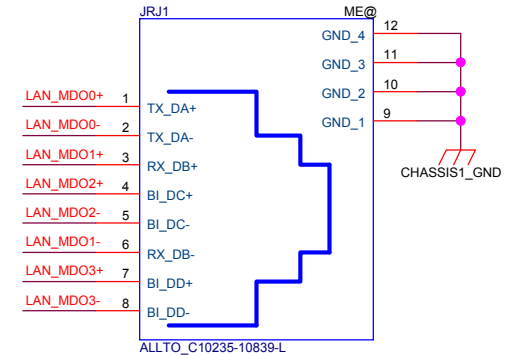
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Title			
LAN_RTL8106E			
Size Custom	Document Number	Rev 1.0	
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DL1/DL2
1'S PN:SC300004X00



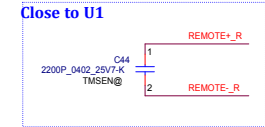
**change TL1 PN SP050008C00 to SP050009G00;
TL1 is SP050008C00 footprint**



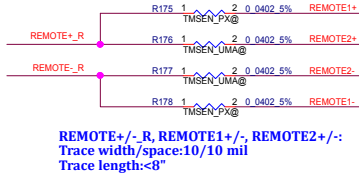
8/16 Update RJ45 P/N DC021608091 wei

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	LAN_Transformer	
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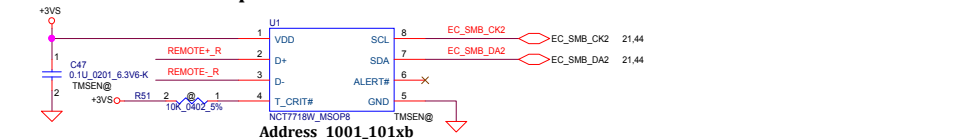
THERMAL SENSOR



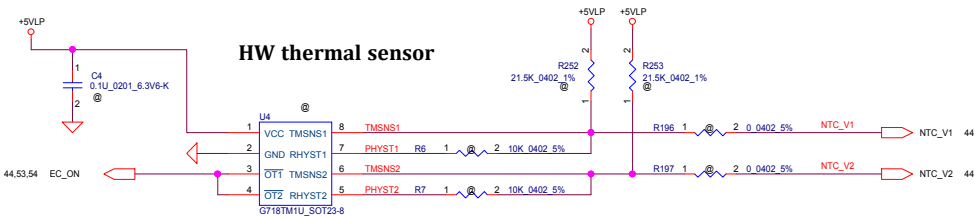
Set Thermal Sensor as a BOM Structure



SMSC thermal sensor placed near DIMM

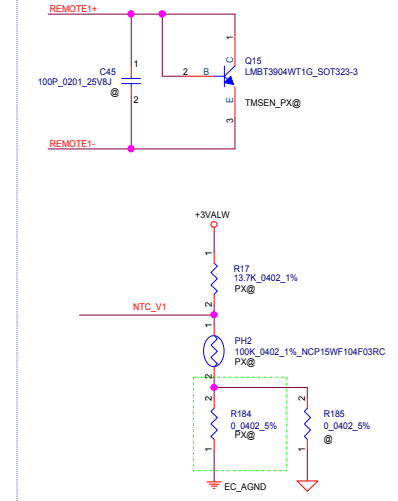


HW thermal sensor

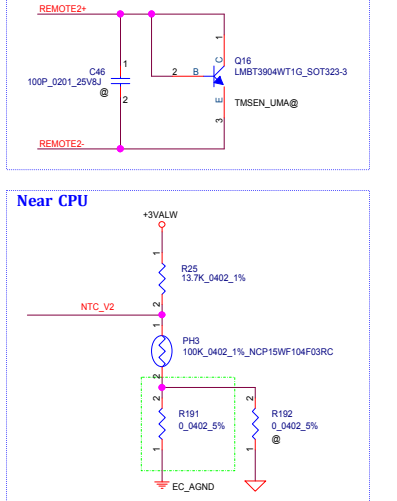


Over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

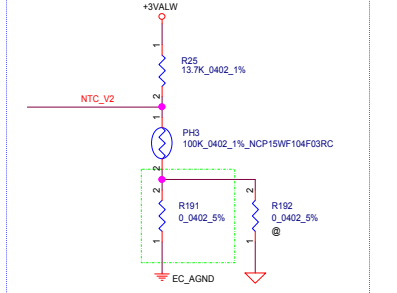
Near GPU&VRAM



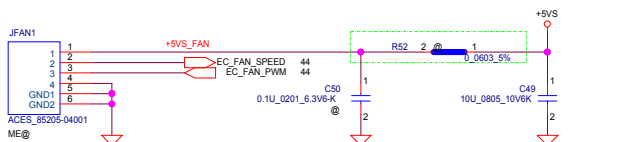
Near CPU Core



Near CPU

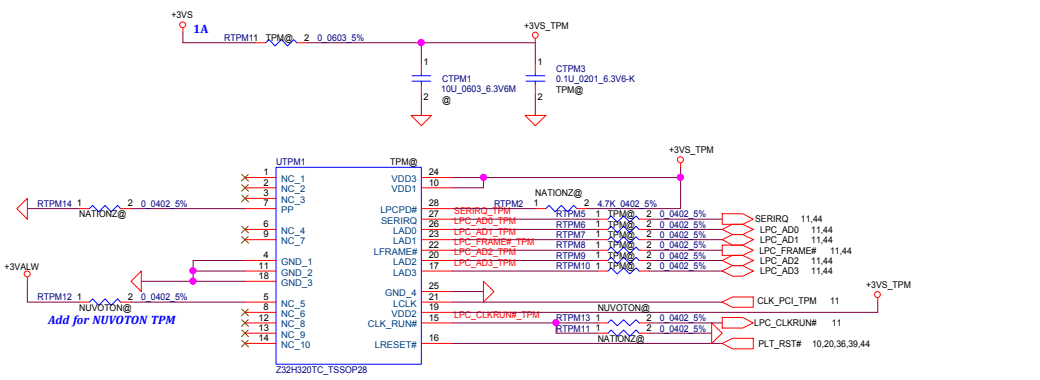


FAN Conn

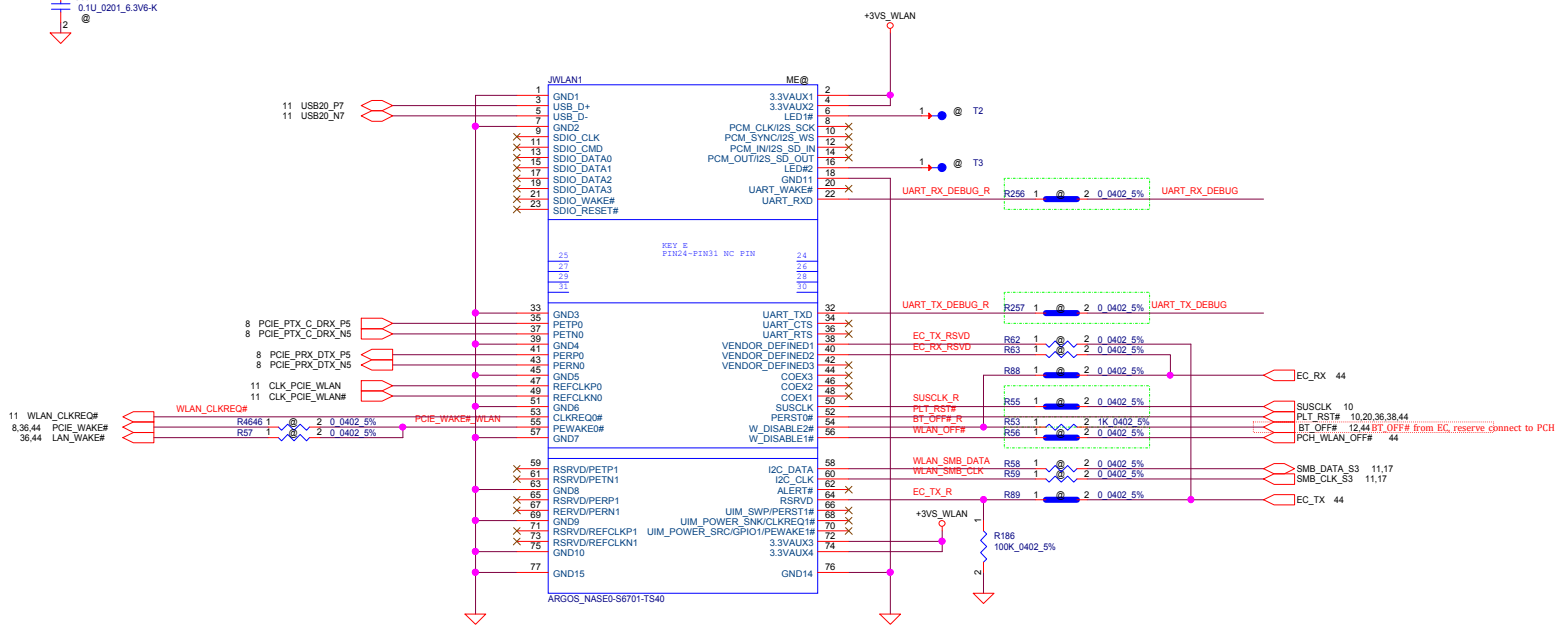
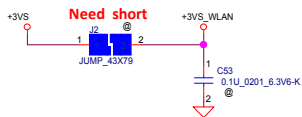


Update FAN conn. footprint to SP020008X0J
SP020012200 main source is SP020008X0J
Lewis 2016/10/14

TPM

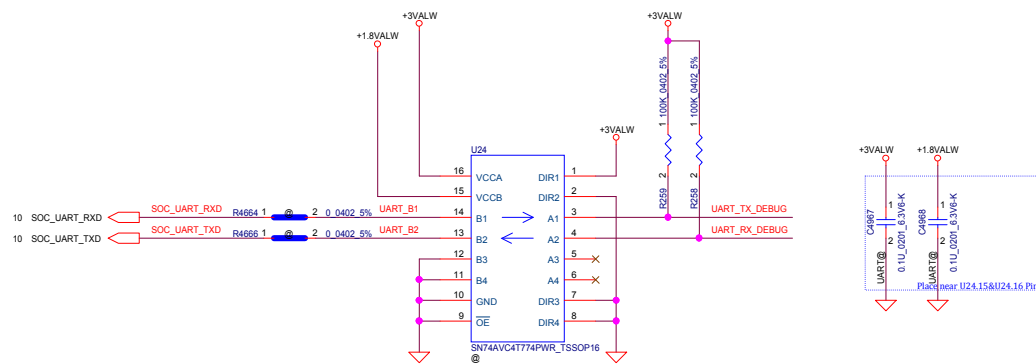



Mini-Express Card(WLAN/WiMAX)



**8/16 Update Conn. P/N SP070013200 wei
Copy DG421 symbol**

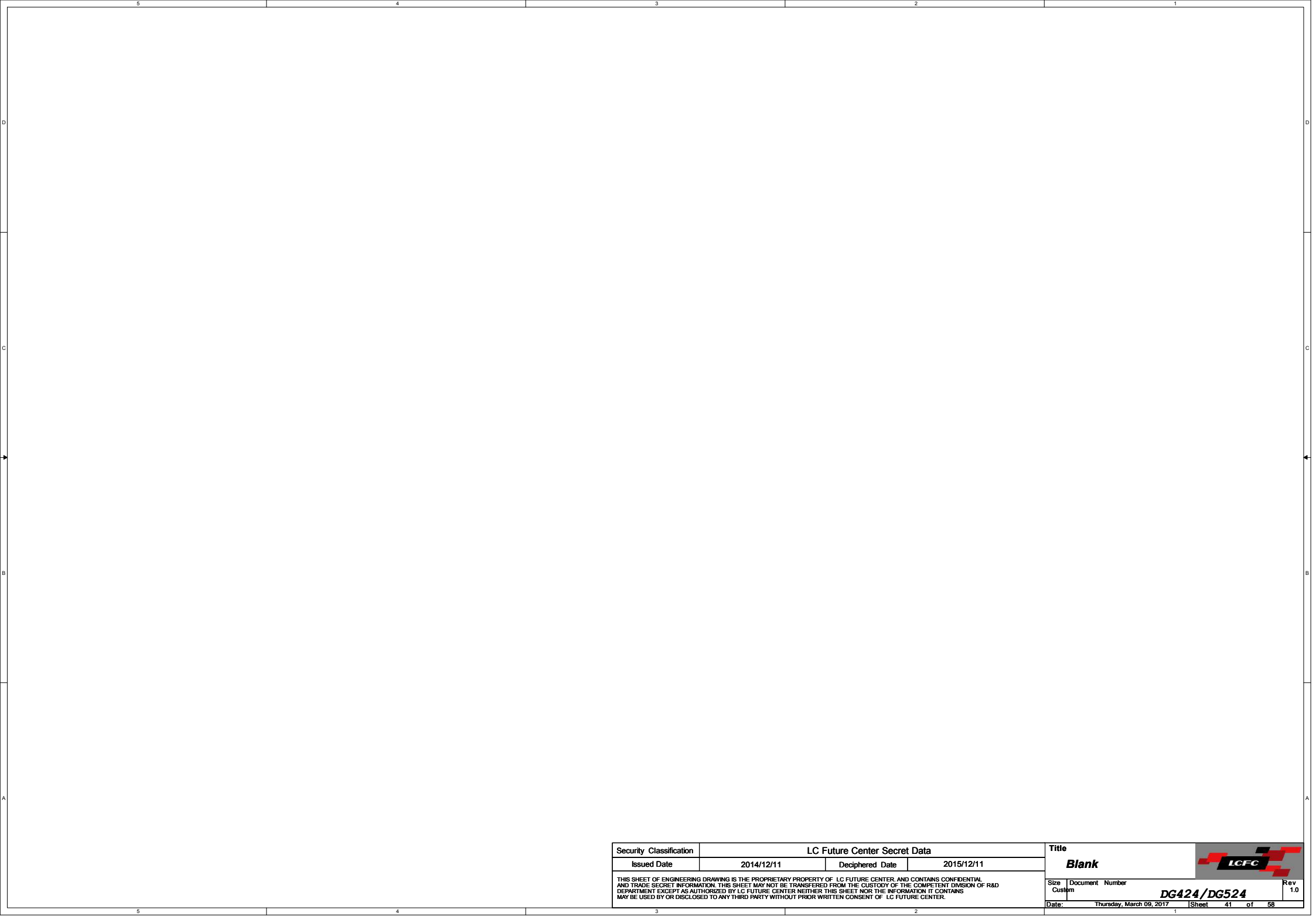
UART Transceiver




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Date: Thursday, March 09, 2017				Sheet	40 of 58

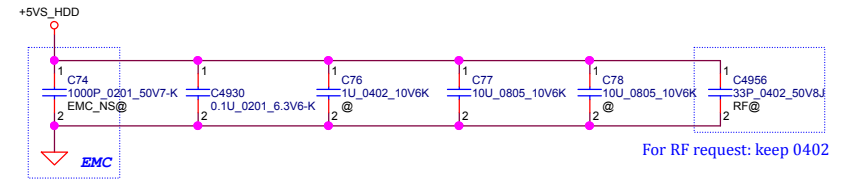
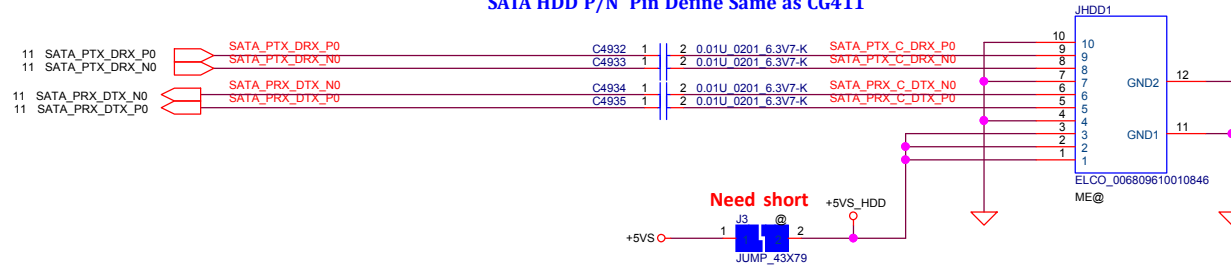




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<small>Date:</small>					<small>Thursday, March 09, 2017</small>			<small>Sheet</small> 41 <small>of</small> 58

SATA HDD Conn.

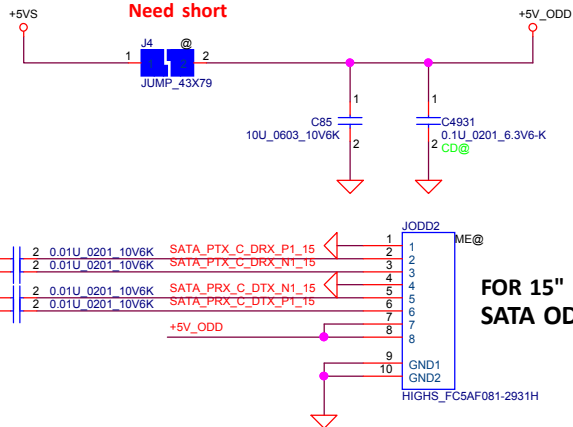
SATA HDD P/N Pin Define Same as CG411



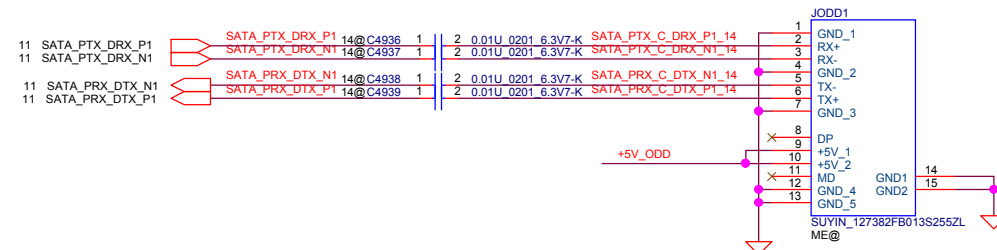
For RF request: keep 0402

+5VS to +5V_ODD


Need short

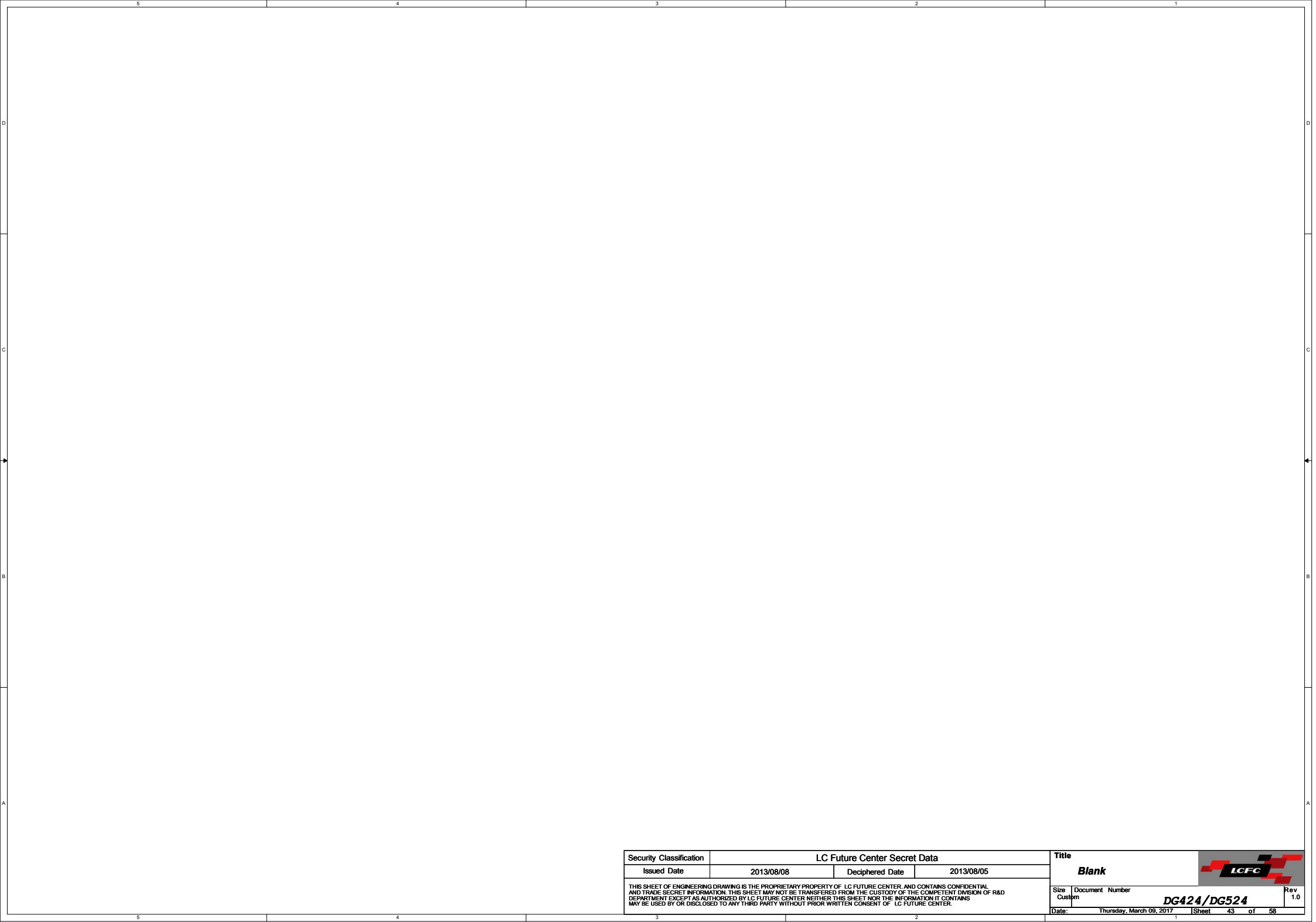


FOR 15"
SATA ODD FFC Conn




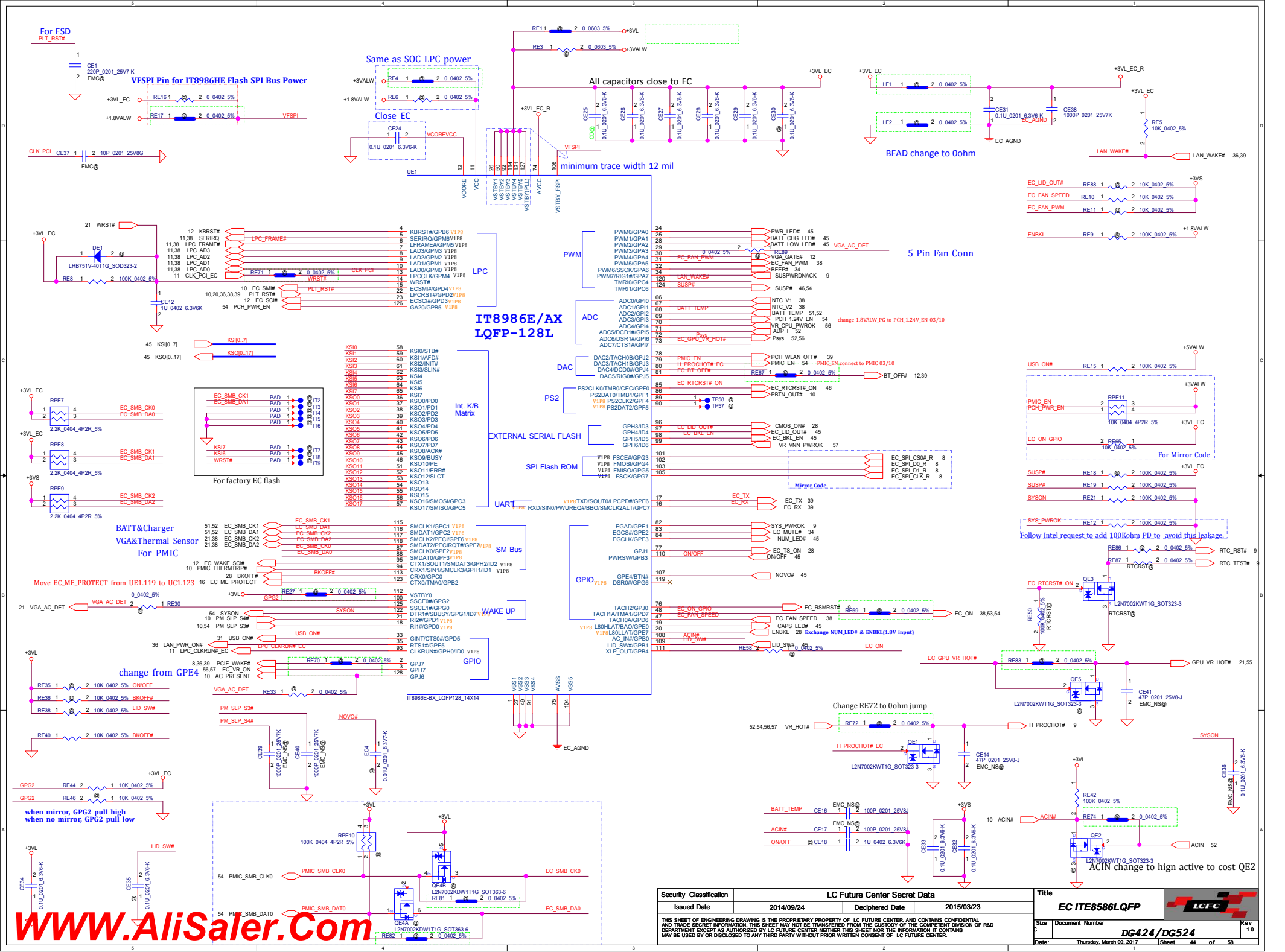
**FOR 14"
SATA ODD Conn.**

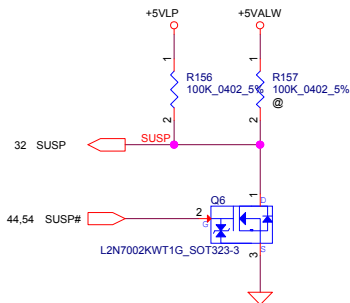
Security Classification		LC Future Center Secret Data		Title			
Issued Date	2013/08/08	Deciphered Date	2013/08/05	HDD/ODD CONN			
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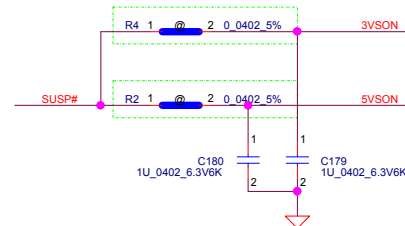
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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+5VS/+3VS Load Switch



Load Switch

+5VALW To +5VS

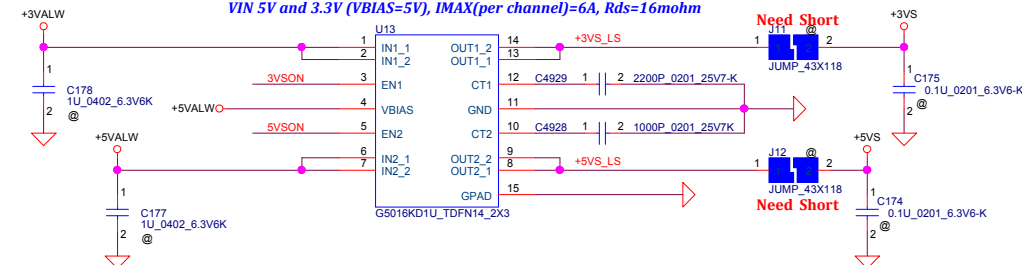
+3VALW To +3VS

modify load swtch from APL3523 to G5016KD1U TDFN 14P

+3VS, C173 --> 2.78ms

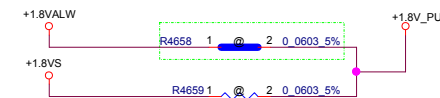
+5VS, C176 --> 1.71ms

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



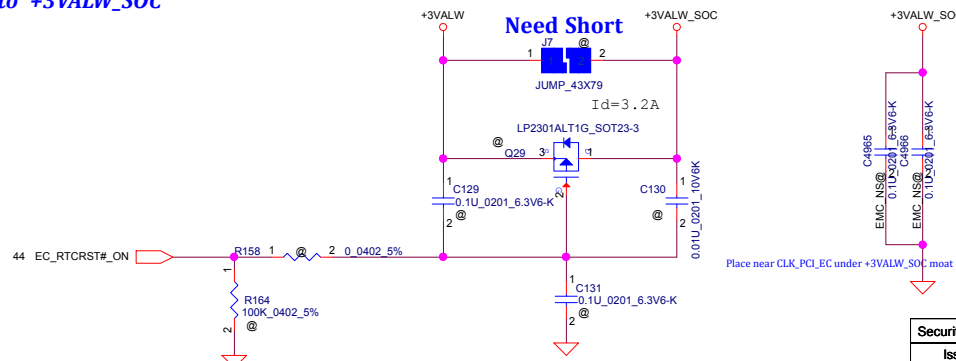
Delete +3.3VALW to +1.5VS

+1.8V_PU Power Rail



+3VALW to +3VALW_SOC

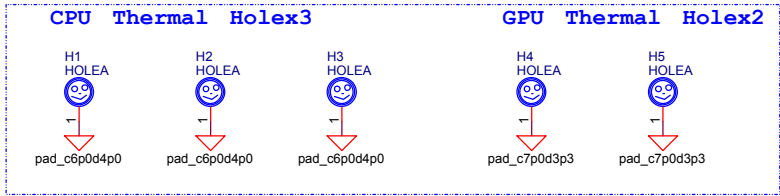
For DisCharge



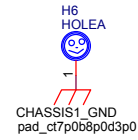
reserve to cut off SOC 3VALW when clear CMOS

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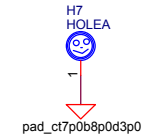
WWW.AliSaler.Com



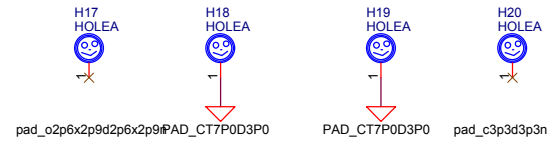
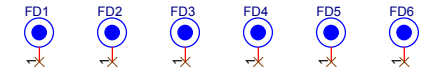
Close to RJ45



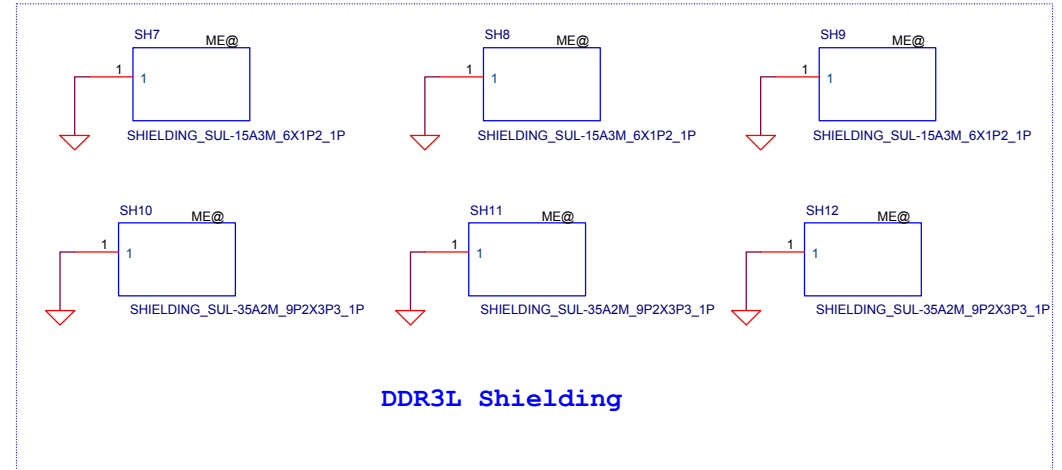
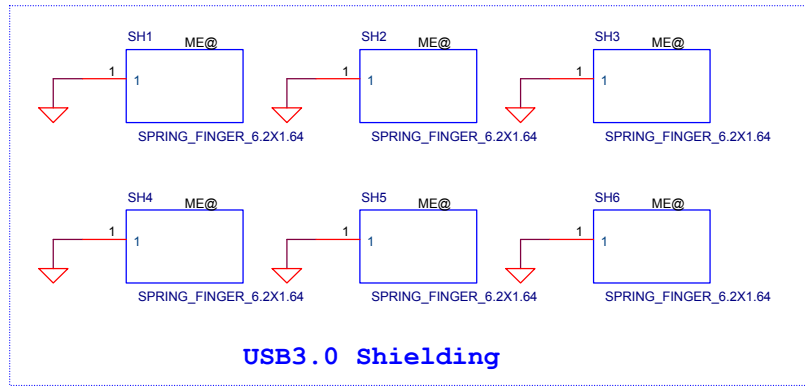
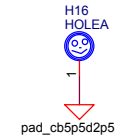
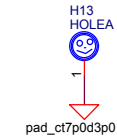
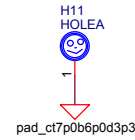
Close to Audio jack



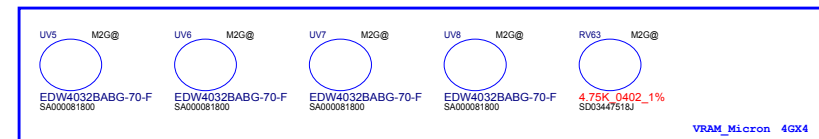
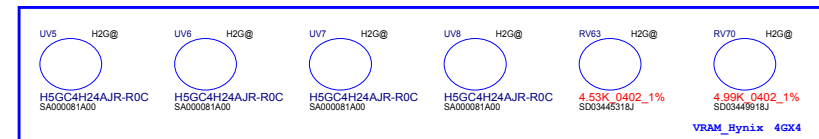
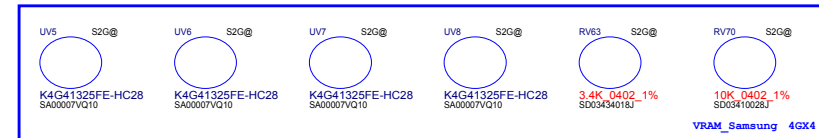
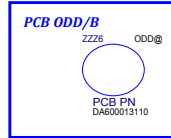
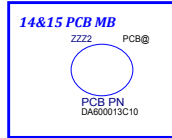
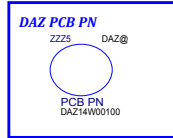
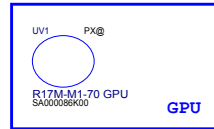
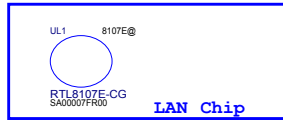
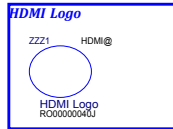
PCB Federal Mark PAD



WLAN Standoff

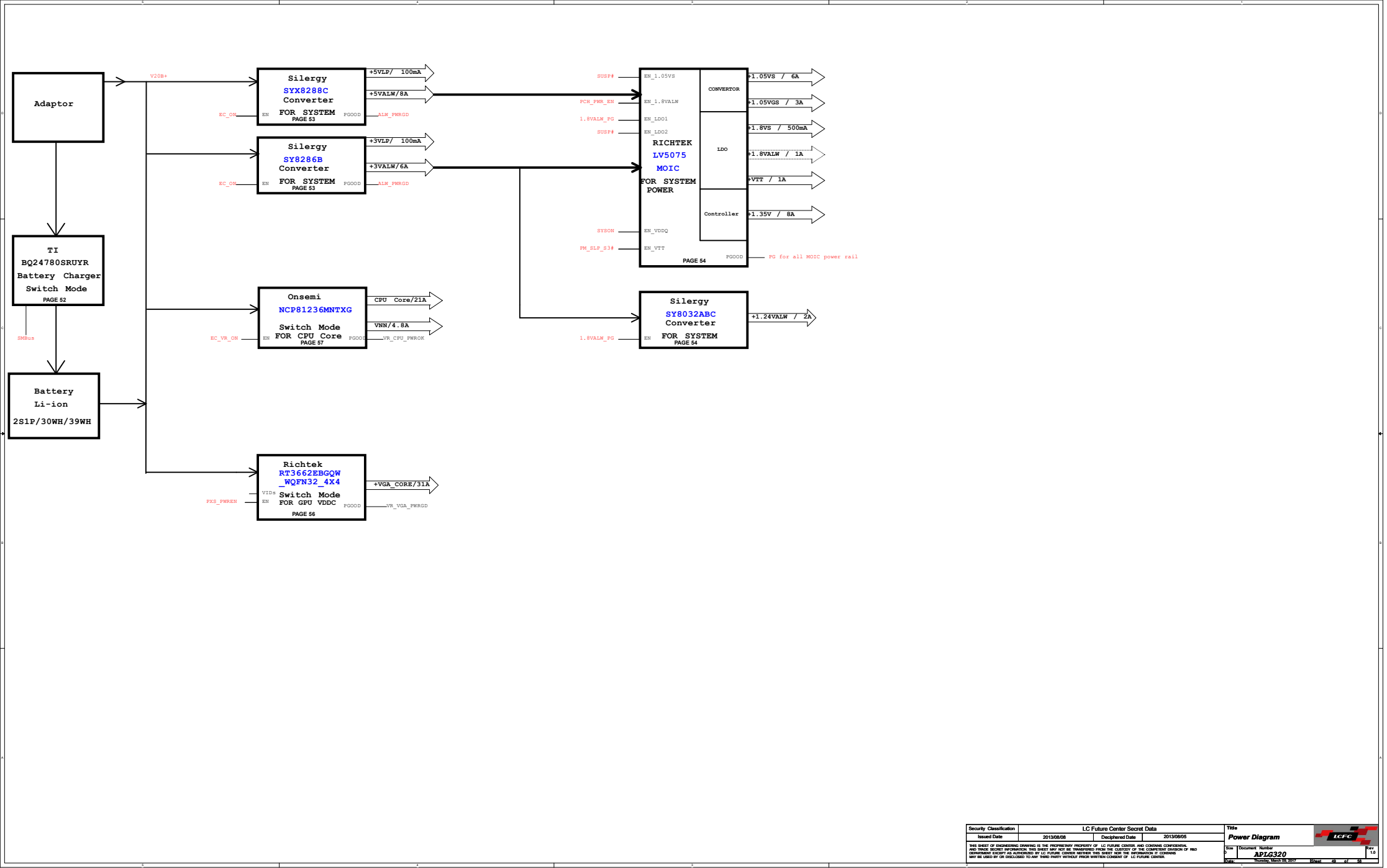


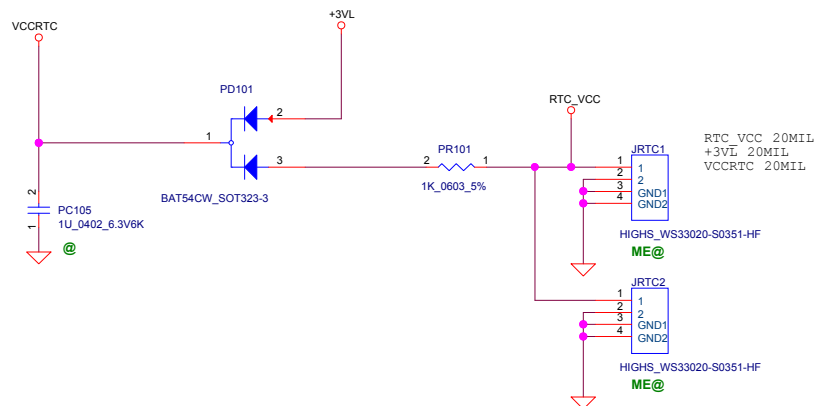
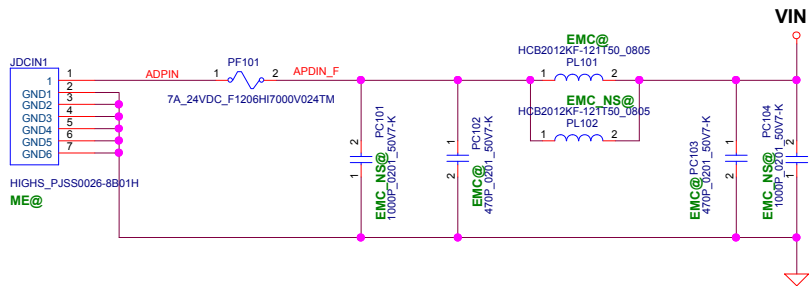
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VRAM ID config

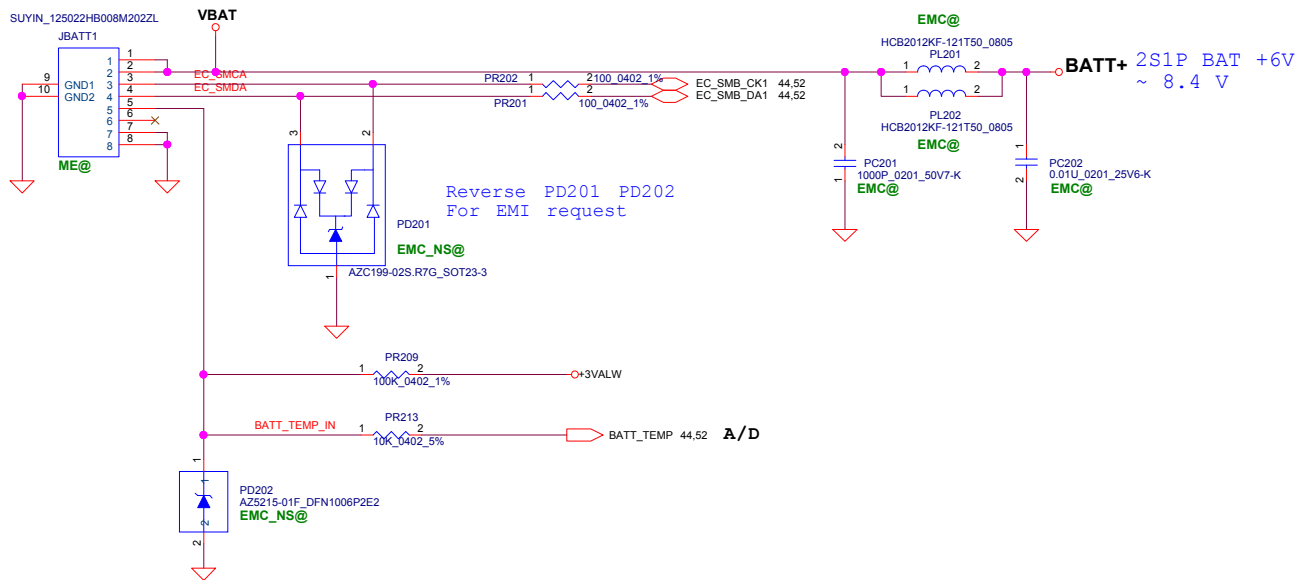
Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
256Mx16	Hynix H5GC4H24AJR-R0C	100	4.53K	4.99K
	Micron EDW4032BABG-70-F	111	4.75K	NC
	Samsung K4G41325FE-HC28	110	3.4K	10K
		000	NC	4.75K
		010	4.53K	2K
		001	8.45K	2K

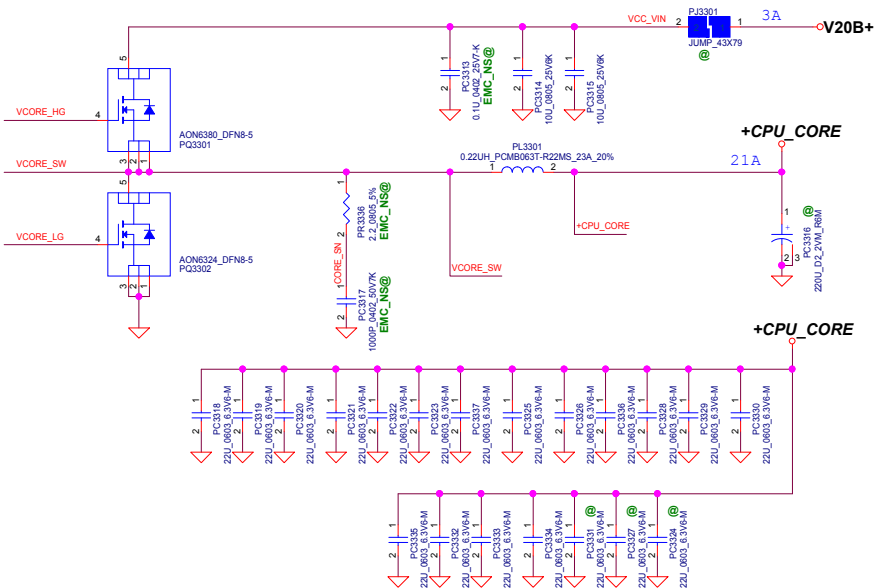
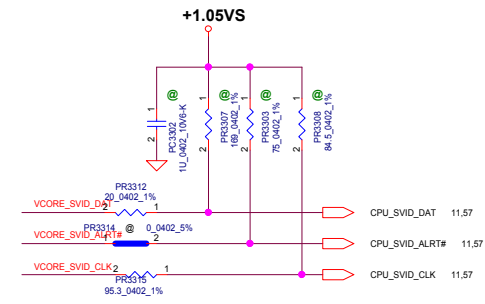
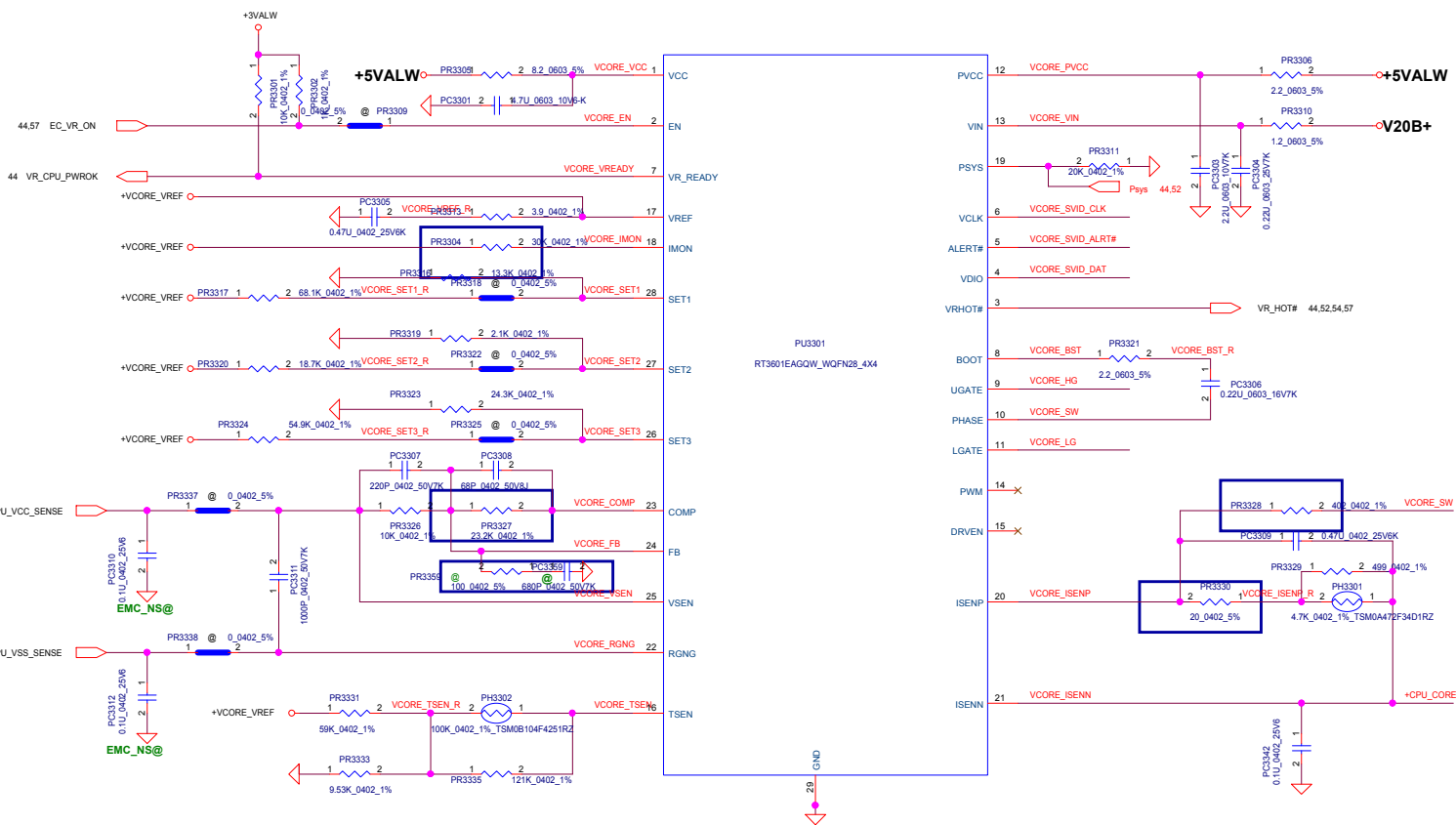




35mm cable
RTC Battery for GCM BOM
(2nd source and quoted price)

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Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-DCIN / RTC charger	
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VID1=1.3V
 Vboot=0V
 DCR=2.5mohm
 TDC/Iccmax=18/21A
 OCP=33.6A
 OVP=Vout+350mV
 Loadline=6mV
 UVP=Vout-300mV
 Fsw=600KHz

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20161216:SDV to SIT
1.p56-p57 add R=100ohm,C=680pF in FB pin;
2.pr3324 change to 55.4kohm,pr3323 change to 24.3k;
3.VNN pr3430 from 0ohm change to 20ohm, pr3428 from 210 change to 249ohm,pr3410 from 34k to 35.7k;
4.Vcore pr3330 from 0ohm change to 20ohm, pr3328 change from 287ohm to 402ohm,pr3327 change from 28.7k to 23.2k, pr3304 change from 24k to 30k;
5. GPU change 14 items to support AMD request.

20161219:SDV to SIT
1.DEL 8pcs MLCC for VNN test result.(PC3422,PC3426,PC3434,PC3436,PC3437,PC3432,PC3435,PC3433)

20161226:SDV to SIT
1. PMIC change 1.24V Vin from 3VALW to1.8VALW;
2.chenge PR2431 from PX@ to @, PR2433 from @ to PX@,
3.change PR734 to @.

20170104:SDV to SIT
1. PMIC change LV5075B TO LV5075A

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